ZL40250–ZL40253 SmartBuffer™

6- or 10-Output Programmable Fanout Buffers with Multi-Format I/O and Dividers

Data Sheet

September 2020

Features

- **Four Flexible Input Clocks**
  - One crystal/CMOS input
  - Two differential/CMOS inputs
  - One single-ended/CMOS input
  - Any input frequency up to 1GHz (300MHz for CMOS)
  - Manual clock switching by pin or register
- **6 or 10 Universal Output Clocks with Dividers**
  - Each output has independent divider
  - Low additive jitter <200fs RMS (12kHz-20MHz, for input frequencies ≥100MHz)
  - Each output configurable as LVDS, LVPECL, HCSL, 2xCMOS or HSTL
  - In 2xCMOS mode, the P and N pins can be different frequencies (e.g. 125MHz and 25MHz)*
  - Multiple output supply voltage banks with CMOS output voltages from 1.5V to 3.3V
  - Precise output alignment circuitry from GPIO pin or register bit*
  - Per-output skew adjustment*
  - Per-output enable/disable and glitchless start/stop (stop high or low) *

Ordering Information

ZL40250LDG1	ext. EEPROM	6 Outputs	Trays
ZL40250LDF1	ext. EEPROM	6 Outputs	Tape and Reel
ZL40251LDG1	int. EEPROM	6 Outputs	Trays
ZL40251LDF1	int. EEPROM	6 Outputs	Tape and Reel
ZL40252LDG1	ext. EEPROM	10 Outputs	Trays
ZL40252LDF1	ext. EEPROM	10 Outputs	Tape and Reel
ZL40253LDG1	int. EEPROM	10 Outputs	Trays
ZL40253LDF1	int. EEPROM	10 Outputs	Tape and Reel

Matte Tin
Package size: 8 x 8 mm, 56 Pin QFN
-40°C to +85°C

- **General Features**
  - Automatic self-configuration at power-up from external (ZL40250 or 2) or internal (ZL40251 or 3) EEPROM; up to 8 configurations pin-selectable
  - PCIe 1, 2, 3, 4 compliant
  - Four multi-purpose I/O pins
  - SPI or I²C processor Interface
  - Core supply voltage options: 2.5V only, 3.3V only, 1.8V+2.5V or 1.8V+3.3V
  - Space-saving 8x8mm QFN56 (0.5mm pitch)
  - Easy-to-use evaluation/programming software

Applications

- Clock signal fanout, format conversion, frequency division and skew adjustment in a wide variety of equipment types

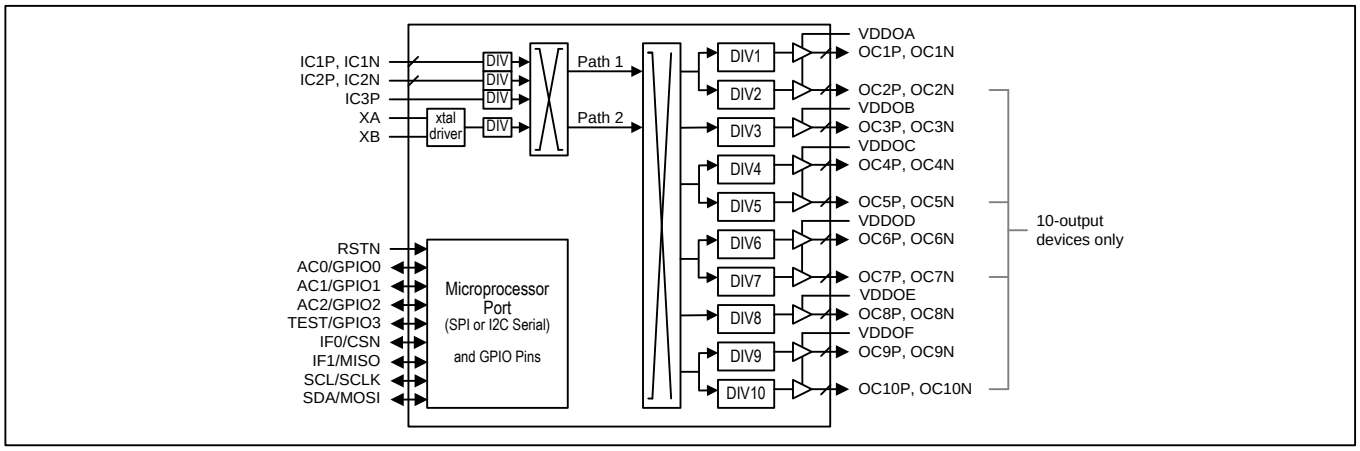


Figure 1 - Functional Block Diagram

* some features require a higher-frequency input clock and enabling the output dividers

Table of Contents

List of Figures

List of Tables

1. Application Examples

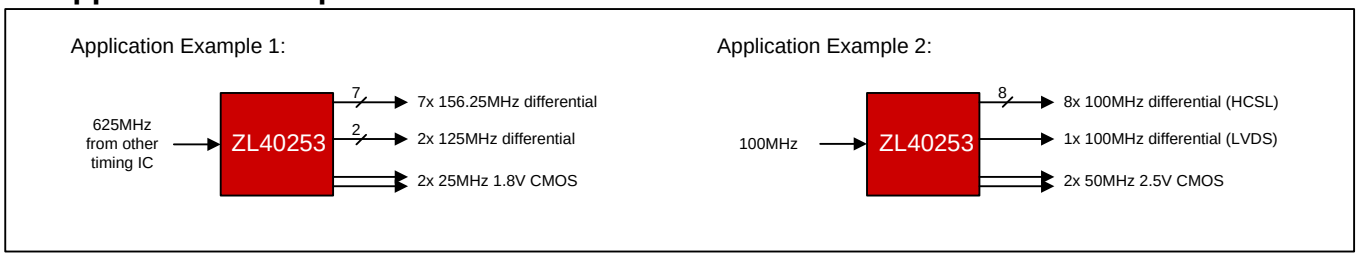


Figure 2 - Application Examples: Ethernet and PCIe Clocks

2. Pin Diagram

The device is packaged in a 8x8mm 56-pin QFN.

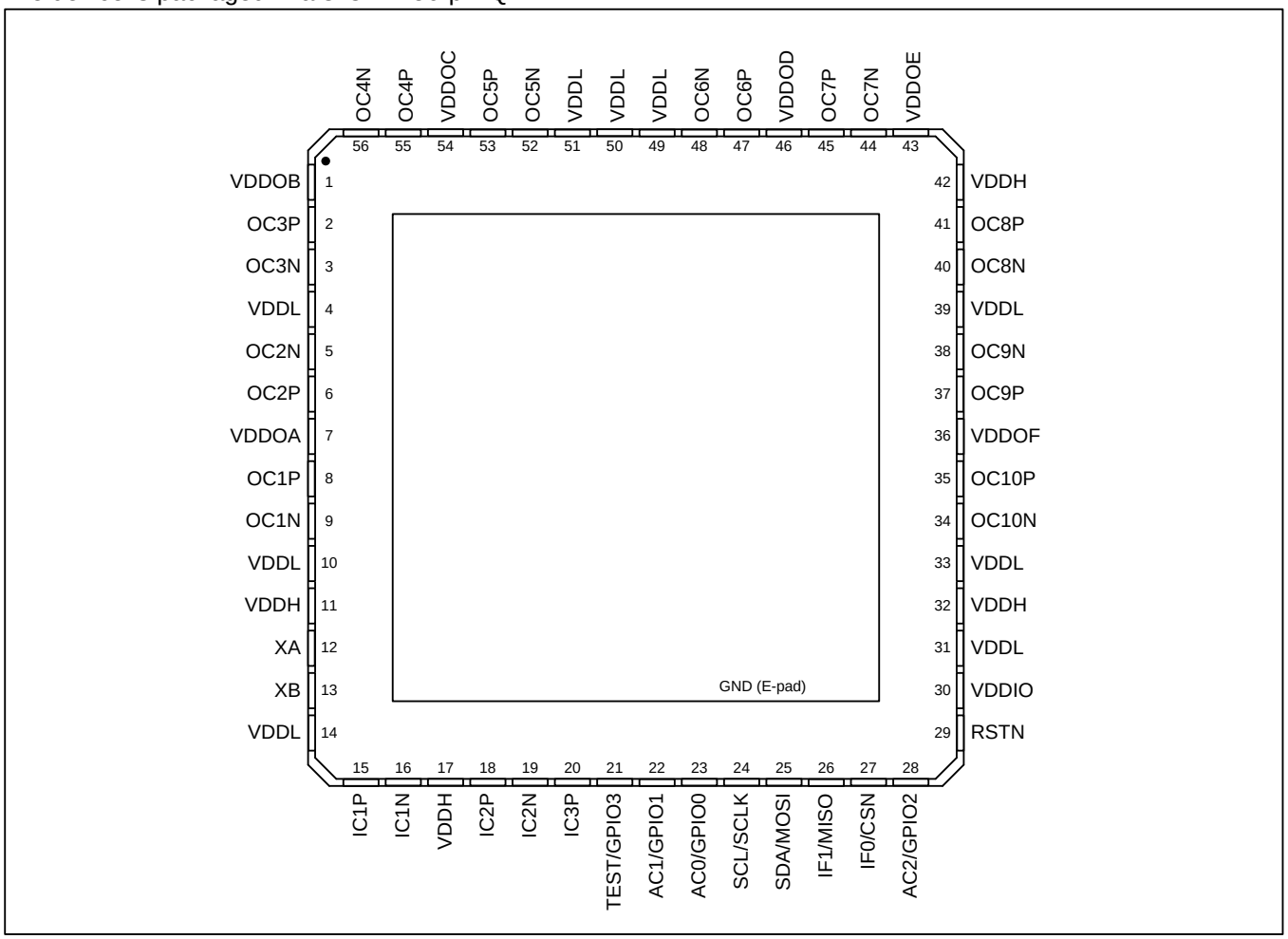


Figure 3 - Pin Diagram

3. Pin Descriptions

All device inputs and outputs are LVCMOS unless described otherwise. The Type column uses the following symbols: I – input, O – output, A – analog, P – power supply pin. All GPIO and SPI/I²C interface pins have Schmitt-trigger inputs and have output drivers that can be disabled (high impedance).

Table 1 - Pin Descriptions

Pin #	Name	Type	Description
15, 16 18, 19 20	IC1P, IC1N IC2P, IC2N IC3P	I I I	**Input Clock Pins** Differential or Single-ended signal format. Programmable frequency. *Differential:* See Table 9 for electrical specifications, and see Figure 14 for recommended external circuitry for interfacing these differential inputs to LVDS, LVPECL, CML or HSCL output pins on neighboring devices. *Single-ended:* For input signal amplitude >2.5V, connect the signal directly to ICxP pin. For input signal amplitude ≤2.5V, AC-coupling the signal to ICxP is recommended. Connect the N pin to a capacitor (0.1µF or 0.01µF) to VSS. As shown in Figure 14, the ICxP and ICxN pins are internally biased to approximately 1.3V. Treat the ICxN pin as a sensitive node; minimize stubs; do not connect to anything else including other ICxN pins. *Unused:* Set ICEN.ICxEN=0. The ICxP and ICxN pins can be left floating. Note that the IC3N pin is not bonded out. A differential signal can be connected to IC3P by AC-coupling the POS trace to IC3P and terminating the signal on the driver side of the coupling cap.
12 13	XA XB	A / I	**Crystal or Input Clock Pins** *Crystal:* MCR2.XAB=01. An on-chip crystal driver circuit is designed to work with an external crystal connected to the XA and XB pins. See section 4.3.2 for crystal characteristics and recommended external components. *Input Clock:* MCR2.XAB=10. An external local oscillator or clock signal can be connected to the XA pin. The XB pin must be left unconnected. The signal on XA can be as large as 3.3V even when VDDH is only 2.5V.
8, 9 6, 5 2, 3 55, 56 53, 52 47, 48 45, 44 41, 40 37, 38 35, 34	OC1P, OC1N OC2P, OC2N OC3P, OC3N OC4P, OC4N OC5P, OC5N OC6P, OC6N OC7P, OC7N OC8P, OC8N OC9P, OC9N OC10P, OC10N	O	**Output Clock Pins** LVDS, programmable differential (which includes LVPECL), HCSL, HSTL or 1 or 2 CMOS. Programmable frequency. Programmable VCM and VOD in programmable differential mode. Programmable drive strength in CMOS and HSTL modes. See Figure 16 for example external interface circuitry. See Table 10, Table 11 and Table 12 for electrical specifications for LVDS, LVPECL and HCSL, respectively. See Table 13 for electrical specifications for interfacing to CMOS and HSTL inputs on neighboring devices. Outputs OC2, OC5, OC7 and OC10 are not present on 6-output products.
29	RSTN	I	**Reset (Active Low)** When this global asynchronous reset is pulled low, all internal circuitry is reset to default values. The device is held in reset as long as RSTN is low. Minimum low time is 1µs.
23 22 28	AC0/GPIO0 AC1/GPIO1 AC2/GPIO2	I/O	**Auto-Configure [2:0] / General Purpose I/O 0, 1 and 2** *Auto Configure:* On the rising edge of RSTN these pins behave as AC[2:0] and specify one of the configurations stored in ROM or EEPROM. See section 4.2.

Pin #	Name	Type	Description
			General-Purpose I/O: After reset these pins are GPIO0, GPIO1 and GPIO2. GPIOCR1 and GPIOCR2.GPIO2C configure these pins. Their states are indicated in GPIOSR which has both real-time and latched status bits. Note that when the power supply arrangement for the device has VDDL=1.8V, during the interval between VDDH ramping and VDDL ramping these pins can briefly behave as an output driving high.
21	TEST/GPIO3	I/O	**Factory Test / General Purpose I/O 3** *Factory Test:* On the rising edge of RSTN the pin behaves as TEST. Factory test mode is enabled when TEST is high. Typically TEST should be low on the rising edge of RSTN, but see section 4.2 for some options where TEST can be high on the rising edge of RSTN. *General-Purpose I/O:* After reset this pin is GPIO3. GPIOCR2.GPIO3C configures the pin. Its state is indicated in GPIOSR which has both real-time and latched status bits. Note that when the power supply arrangement for the device has VDDL=1.8V, during the interval between VDDH ramping and VDDL ramping this pin can briefly behave as an output driving high.
27	IF0/CSN	I/O	**Interface Mode 0 / SPI Chip Select (Active Low)** *Interface Mode:* On the rising edge of RSTN the pin behaves as IF0 and, together with IF1, specifies the interface mode for the device. See section 4.2. *SPI Chip Select:* After reset this pin is CSN. When the device is configured as a SPI slave, an external SPI master must assert (low) CSN to access device registers. When the device is configured as a SPI master (ZL40250, ZL40252 only), the device asserts CSN to access an external SPI EEPROM during auto-configuration and then changes CSN to an input during normal operation. CSN should not be allowed to float.
26	IF1/MISO	I/O	**Interface Mode 1 / SPI Master-In-Slave-Out** *Interface Mode:* On the rising edge of RSTN the pin behaves as IF1 and, together with IF0, specifies the interface mode for the device. See section 4.2. *SPI MISO:* After reset this pin is MISO. When the device is configured as a SPI slave, the device outputs data to an external SPI master on MISO during SPI read transactions. When the device is configured as a SPI master (ZL40250, ZL40252 only), the device receives data on MISO from an external SPI EEPROM during auto-configuration.
24	SCL/SCLK	I/O	**I^2C Clock / SPI Clock** *I^2C Clock:* When the device is configured as an I^2C slave, an external I^2C master must provide the I^2C clock signal on the SCL pin. In I^2C mode this pin should be externally pulled high by a 1kΩ to 5kΩ resistor. *SPI Clock:* When the device is configured as a SPI slave, an external SPI master must provide the SPI clock signal on SCLK. When the device is configured as a SPI master (ZL40250, ZL40252 only), the device drives SCLK as an output to clock accesses to an external SPI EEPROM during auto-configuration.
25	SDA/MOSI	I/O	**I^2C Data / SPI Master-Out-Slave-In** *I^2C Data:* When the device is configured as an I^2C slave, SDA is the

Pin #	Name	Type	Description
			bidirectional data line between the device and an external I²C master. In I²C mode this pin should be externally pulled high by a 1kΩ to 5kΩ resistor. *SPI MOSI:* When the device is configured as a SPI slave, an external SPI master sends commands, addresses and data to the device on MOSI. When the device is configured as a SPI master (ZL40250, ZL40252 only), the device sends commands, addresses and data on MOSI to an external SPI EEPROM during auto-configuration.
11,17, 32,42	VDDH	P	**Higher Core Power Supply.** 2.5V or 3.3V ±5%. When VDDH=3.3V the device has additional internal power supply regulators enabled.
4,10, 14,31, 33,39, 49,50, 51	VDDL	P	**Lower Core Power Supply.** 1.8V ±5% or same voltage as VDDH.
30	VDDIO	P	**Digital Power Supply for Non-Clock I/O Pins.** 1.8V to VDDH.
7	VDDOA	P	**Power Supply for OC1P/N and OC2P/N.** 1.5V to VDDH.
1	VDDOB	P	**Power Supply for OC3P/N.** 1.5V to VDDH.
54	VDDOC	P	**Power Supply for OC4P/N and OC5P/N.** 1.5V to VDDH.
46	VDDOD	P	**Power Supply for OC6P/N and OC7P/N.** 1.5V to VDDH.
43	VDDOE	P	**Power Supply for OC8P/N.** 1.5V to VDDH.
36	VDDOF	P	**Power Supply for OC9P/N and OC10P/N.** 1.5V to VDDH.
E-pad	VSS	P	**Ground.** 0 Volts.

Important Note: The voltages on VDDL, VDDIO, and all VDDOx pins must not exceed VDDH. Not complying with this requirement may damage the device.

4. Functional Description

4.1 Device Identification

The 12-bit read-only ID field and the 4-bit revision field are found in the ID1 and ID2 registers. Contact the factory to interpret the revision value and determine the latest revision.

4.2 Pin-Controlled Automatic Configuration at Reset

The device configuration is determined at reset (i.e. on the rising edge of RSTN) by the signal levels on these device pins: TEST/GPIO3, AC2/GPIO2, AC1/GPIO1, AC0/GPIO0, IF1/MISO and IF0/CSN. For these pins, the first name (TEST, AC2, AC1, AC0, IF1, IF0) indicates their function when they are sampled by the rising edge of the RSTN pin. The second name refers to their function after reset. The values of these pins are latched into the CFGSR register when RSTN goes high. To ensure the device properly samples the reset values of these pins, the following guidelines should be followed:

1. Any pullup or pulldown resistors used to set the value of these pins at reset should be 1kΩ.
2. RSTN must be asserted at least as long as specified in section 4.9.

The hardware configuration pins are grouped into three sets:

1. TEST - Manufacturing test mode
2. IF[1:0] – Microprocessor interface mode and I²C address
3. AC[2:0] – Auto-config configuration number (0 to 7)

The TEST pin selects manufacturing test modes when TEST=1 (the AC[2:0] pins specify the test mode). For ZL40251 and ZL40253 (devices with internal EEPROM), TEST=1, AC[2:0]=000, IF[1:0]=11 configures the part so that production SPI EEPROM programmers can program the internal EEPROM (see section 4.11.2). TEST=1 and AC[2:0]=011 causes the part to start normally except it does not auto-configure from EEPROM or ROM. For more information about auto-configuration from EEPROM or ROM see section 4.11.

For all of these pins Microsemi recommends that board designs include component sites for both pullup and pulldown resistors (only one or the other populated per pin).

4.2.1 ZL40250 and ZL40252—Internal ROM, External or No EEPROM

For these part numbers the IF[1:0] pins specify the processor interface mode, the I²C slave address and whether the device should auto-configure from internal ROM or external EEPROM. The AC[2:0] pins specify which device configuration in the ROM or EEPROM to execute after reset. Descriptions of the standard-product ROM configurations are available from Microsemi.

IF1	IF0	Processor Interface	Configuration Memory to Use
0	0	I²C, slave address 11101 00	Internal ROM
0	1	I²C, slave address 11101 01	Internal ROM
1	0	SPI Slave	Internal ROM
1	1	SPI Master during auto-configuration then SPI Slave	External SPI EEPROM

To configure the device as specified in the first three rows above but *without* auto-configuring from internal ROM, wire devices pins as follows: TEST=1 and AC[2:0]=011, as described in section 4.2.

AC2	AC1	AC0	Auto Configuration
0	0	0	Configuration 0
0	0	1	Configuration 1
0	1	0	Configuration 2
0	1	1	Configuration 3
1	0	0	Configuration 4
1	0	1	Configuration 5
1	1	0	Configuration 6
1	1	1	Configuration 7

Notes about the device auto-configuring from external EEPROM:

1. The device's CSN pin should have a pull-up resistor to VDD to ensure its processor interface is inactive after auto-configuration is complete. The SCLK, MISO and MOSI pins should also have pull-up resistors to VDD to keep them from floating.
2. If a processor or similar device will access device registers after the device has auto-configured from external EEPROM, the SPI SCLK, MOSI and MISO wires can be connected directly to the processor, the device and the external EEPROM. The processor and device CSN pins can be wired together also. The EEPROM CSN signal must be controlled by the device's CSN pin during device auto-configuration and then held inactive when the processor accesses device registers.
3. The bits of the I²C address are as shown above by default but can be changed in the I2CA register.

4.2.2 ZL40251 and ZL40253—Internal EEPROM

For these part numbers the IF[1:0] pins specify the processor interface mode and the I²C slave address. The AC[2:0] pins specify which device configuration in the EEPROM to execute after reset.

IF1	IF0	Processor Interface
0	0	I²C, slave address 11101 00
0	1	I²C, slave address 11101 01
1	0	I²C, slave address 11101 10
1	1	SPI Slave

AC2	AC1	AC0	Auto Configuration
0	0	0	Configuration 0
0	0	1	Configuration 1
0	1	0	Configuration 2
0	1	1	Configuration 3
1	0	0	Configuration 4

AC2	AC1	AC0	Auto Configuration
1	0	1	Configuration 5
1	1	0	Configuration 6
1	1	1	Configuration 7

Note: the bits of the I²C address are as shown above by default but can be changed in the I2CA register. A device's I²C slave address can be set to any value during auto-configuration at power-up by writing the I2CA register as part of the configuration script.

4.3 Local Oscillator or Crystal

Section 4.3.1 describes how to connect an external oscillator and the required characteristics of the oscillator. Section 4.3.2 describes how to connect an external crystal to the on-chip crystal driver circuit and the required characteristics of the crystal. The device does not require an external oscillator or crystal for operation.

4.3.1 External Oscillator

A signal from an external oscillator can be connected to the XA pin (XB must be left unconnected).

Table 8 specifies the range of possible frequencies for the XA input. To minimize jitter, the signal must be properly terminated and must have very short trace length. A poorly terminated single-ended signal can greatly increase output jitter, and long single-ended trace lengths are more susceptible to noise. When MCR2.XAB=10, XA is enabled as a single-ended input.

4.3.2 External Crystal and On-Chip Driver Circuit

The on-chip crystal driver circuit is designed to work with a fundamental mode, AT-cut crystal resonator. See Table 2 for recommended crystal specifications. To enable the crystal driver, set MCR2.XAB=01.

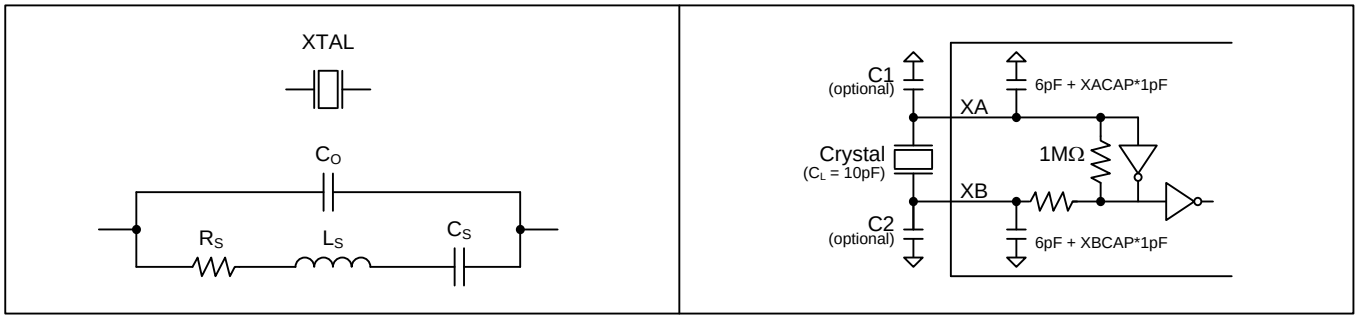


Figure 4 - Crystal Equivalent Circuit / Recommended Crystal Circuit

See Figure 4 for the crystal equivalent circuit and the recommended external component connections. The driver circuit design includes configurable internal load capacitors. For a 10pF crystal the total capacitance on each of XA and XB should be 2 x 10pF = 20pF. To achieve these loads without external capacitors, register field XACR3.XACAP should be set to 20pF minus actual XA external board trace capacitance minus XA's minimum internal capacitance of 6pF. For example, if external trace capacitance is 2pF then XACAP should be set to 20pF – 2pF – 6pF = 12pF. Register field XACR3.XBCAP should be set in a similar manner for XB load capacitance. Crystals with nominal load capacitance other than 10pF usually can be supported with only internal load capacitance. If the XACAP and XBCAP fields do not have sufficient range for the application, capacitance can be increased by using external caps C1 and C2.

Users should also note that on-chip capacitors are not nearly as accurate as discrete capacitors (which can have 1% accuracy). If tight frequency accuracy is required for the crystal driver circuit then set XACAP and XBCAP both to 0 and choose appropriate C1 and C2 capacitors with 1% tolerance.

The crystal, traces, and two external capacitors sites (if included) should be placed on the board as close as possible to the XA and XB pins to reduce crosstalk of active signals into the oscillator. Also no active signals should be routed under the crystal circuitry.

Note: Crystals have temperature sensitivities that can cause frequency changes in response to ambient temperature changes. In applications where significant temperature changes are expected near the crystal, it is recommended that the crystal be covered with a thermal cap, or an external XO or TCXO should be used instead.

Table 2 - Crystal Selection Parameters

Parameter		Symbol	Min.	Typ.	Max.	Units
Crystal Oscillation Frequency[1]		f_{OSC}	25		60	MHz
Shunt Capacitance		C_O		2	5	pF
Load Capacitance[3]		C_L	8	10	16	pF
Equivalent Series Resistance (ESR)[2]	f_{OSC} < 40MHz	R_S			60	Ω
	f_{OSC} > 40MHz	R_S			50	Ω
Maximum Crystal Drive Level			100	100, 200, 300		µW

Note 1: Higher frequencies give lower output jitter, all else being equal.

Note 2: These ESR limits are chosen to constrain crystal drive level to less than 100µW. If the crystal can tolerate a drive level greater than 100µW then proportionally higher ESR is acceptable.

Note 3: For crystals with 100µW max drive level: (a) f_{OSC}>55MHz and C_L≥12pF is not supported, and (b) f_{OSC}>45MHz and C_L≥16pF is not supported. Crystals with max drive level of 200µW or higher do not have these limitations.

Parameter	Symbol	Min.	Typ.	Max.	Units
Crystal Frequency Stability vs. Power Supply	f_{FVD}		0.2	0.5	ppm per 10% Δ in VDD

4.3.3 Ring Oscillator (for Auto-Configuration)

After reset the internal auto-configuration boot controller is clocked by an internal ring oscillator. After auto-configuration is complete (GLOBISR.BCDONE=1) the ring oscillator can be disabled by setting MCR1.ROSCD=1. The device's processor interface is asynchronous and does not require the ring oscillator.

4.4 Input Signal Format Configuration

Input clocks IC1, IC2 and IC3 are enabled by setting the enable bits in the ICEN register. The power consumed by a differential receiver is shown in Table 6. The electrical specifications for these inputs are listed in Table 9. Each input clock can be configured to accept nearly any differential signal format by using the proper set of external components (see Figure 14). To configure these differential inputs to accept single-ended CMOS signals, connect the single-ended signal to the ICxP pin, and connect the ICxN pin to a capacitor (0.1µF or 0.01µF) to VSS. Each ICxP and ICxN pin is internally biased to approximately 1.3V. If an input is not used, both ICxP and ICxN pins can be left floating. Note that the IC3N pin is not present. A differential signal can be connected to IC3P by AC-coupling the POS trace to IC3P and terminating the signal on the driver side of the coupling cap.

4.5 Path 1 and Path 2 Signal Selection

The device has two internal fanout paths, each with its own input mux. See the block diagram in Figure 1. Each bank of outputs can be connected to either path using the appropriate field in the OCMUX registers.

The Path 1 input mux can select any of inputs IC1 through IC3, a clock signal on XA, or the crystal driver circuit when a crystal is connected to XA and XB. The input to Path 1 can be controlled by a register field or a GPIO pin. When P1CR3.EXTSW=0, the P1CR3.MUX register field controls the Path 2 input mux.

When P1CR3.EXTSW=1, a GPIO pin controls the Path 1 input mux. When the GPIO pin is low, the mux selects the input specified by P1CR3.MUX. When the GPIO pin is high, the mux selects the input specified by P1CR3.ALTMUX. P1CR1.EXTSS specifies which GPIO pin controls this behavior.

The P1SR.SELREF real-time status field indicates Path 2's selected reference.

Path 2 has identical register fields to those of Path 1 in the P2CR1, P2CR3 and P2SR registers.

4.6 Output Clock Configuration

The ZL40250 and ZL40251 have six output clock signal pairs while the ZL40252 and ZL40253 have ten. Each output has individual divider, enable and signal format controls. In CMOS mode each signal pair can become two

CMOS outputs, allowing the device to have up to 12 or 20 output clock signals. Also in CMOS mode, the OCxN pin can have an additional divider allowing the OCxN frequency to be an integer divisor of the OCxP frequency (example: OC3P 125MHz and OC3N 25MHz). The outputs can be aligned relative to each other, and the phases of output signals can be adjusted dynamically with high resolution.

4.6.1 Output Enable, Signal Format, Voltage and Interfacing

To use an output, the output driver must be enabled by setting OCxCR2.OCSF≠0, and the per-output dividers must be enabled by setting the appropriate bit in the OCEN register. The per-output dividers include the medium-speed divider, the low-speed divider and the associated phase adjustment/alignment circuitry and start/stop logic.

Using the OCxCR2.OCSF register field, each output pair can be disabled or configured as LVDS, LVPECL, HCSL, HSTL, or one or two CMOS outputs. When an output is disabled it is high impedance, and the output driver is in a low-power state. In CMOS mode, the OCxN pin can be disabled, in-phase or inverted vs. the OCxP pin. All of these options are specified by OCxCR2.OCSF. The clock to the output driver can inverted by setting OCxCR2.POL=1. The CMOS/HSTL output driver can be set to any of four drive strengths using OCxCR2.DRIVE.

When OCxCR2.OCSF=0001 the output driver is in LVDS mode. V_{OD} is forced to 400mV and OCxDIFF.VOD is ignored. V_{CM} can be configured in OCxDIFF.VCM, but the default value of 0000 is typically used to get V_{CM}=1.23V for LVDS.

When OCxCR2.OCSF=0010 the output driver is in programmable differential mode. In this mode the output swing (V_{OD}) can be set in OCxDIFF.VOD and the common-mode voltage can be set in OCxDIFF.VCM. Together these fields allow the output signal to be customized to meet the requirements of the clock receiver and minimize the need for external components. By default, when OCSF=0010 the output is configured for LVPECL signal swing with a 1.23V common mode voltage. This gives a signal that can be AC-coupled (after a 100Ω termination resistor) to receivers that are LVPECL or that require a larger signal swing than LVDS. The output driver can also be configured for LVPECL output with standard 2.0V common-mode voltage by seting OCxDIFF.VCM for 2.0V and setting OCxREG.VREG appropriately.

In both LVDS mode and programmable differential mode the output driver requires a DC path through a 100Ω resistor between OCxP and OCxN for proper operation. This resistor is usually placed as close as possible to the receiver inputs to terminate the differential signal. If the receiver requires a common-mode voltage that cannot be matched by the output driver then the POS and NEG signals can be AC-coupled to the receiver after the 100Ω resistor.

HCSL mode requires a DC path through a 50Ω resistor to ground on each of OCxP and OCxN. Note that each of the OCxDIFF.VCM, OCxDIFF.VOD and OCxREG.VREG register fields has a particular setting required for HCSL signal format. See the descriptions of these fields for details.

Outputs are grouped into six power supply banks, VDDOA through VDDOF to allow CMOS or HSTL signal swing from 1.5V to 3.3V for glueless interfacing to neighboring components. 10-output products have outputs grouped into banks in a 2-1-2-2-1-2 arrangement, as shown in Figure 1. 6-output products have one output per bank. If OCSF is set to HSTL mode then a 1.5V power supply voltage should be used to get a standards-compliant HSTL output. Note that LVDS, LVPECL and HCSL signal formats must have a power supply of 2.5V or 3.3V. Also note that VDDO voltage must not exceed VDDH voltage.

4.6.2 Output Frequency Configuration

The frequency of each output is determined by the output bank source signal and the per-output dividers. Each bank of outputs can be connected to Path 1 or Path 2 using the appropriate field in the OCMUX registers.

Each output has two output dividers, a 7-bit medium-speed divider (OCxCR1.MSDIV) and a 24-bit low-speed output divider (LSDIV field in the OCxDIV registers). These dividers are in series, medium-speed divider first then output divider. These dividers produce signals with 50% duty cycle for all divider values including odd numbers. The low-speed divider can only be used if the medium-speed divider is used (i.e. OCxCR1.MSDIV>0). The maxium input frequency to the medium-speed divider is 750MHz.

Since each output has its own independent dividers, the device can output families of related frequencies that have a path frequency as a common multiple. For example, for Ethernet clocks, a 625MHz Path 1 clock can be divided

by four for one output to get 156.25MHz, divided by five for another output to get 125MHz, and divided by 25 for another output to get 25MHz. Similarly, for SDH/SONET clocks, a 622.08MHz Path 1 clock can be divided by 4 to get 155.52MHz, by 8 to get 77.76MHz, by 16 to get 38.88MHz or by 32 to get 19.44MHz.

Two Different Frequencies in 2xCMOS Mode

When an output is in 2xCMOS mode it can be configured to have the frequency of the OCxN clock be an integer divisor of the frequency of the OCxP clock. Examples of where this can be useful:

- 125MHz on OCxP and 25MHz on OCxN for Ethernet applications
- 77.76MHz on OCxP and 19.44MHz on OCxN for SONET/SDH applications
- 25MHz on OCxP and 1Hz (i.e. 1PPS) on OCxN for telecom applications with Synchronous Ethernet and IEEE1588 timing

An output can be configured to operate like this by setting the LSDIV value in the OCxDIV registers to OCxP_freq / OCxN_freq - 1 and setting OCxCR3.LSSEL=0 and OCxCR3.NEGLSD=1. Here are some notes about this dual-frequency configuration option:

- In this mode only the medium speed divider is used to create the OCxP frequency. The low-speed divider is then used to divide the OCxP frequency down to the OCxN frequency. This means that the lowest OCxP frequency is the bank source frequency divided by 128.
- An additional constraint is that the medium-speed divider must be configured to divide by 2 or more (i.e. must have OCxCR1.MSDIV≥1).

4.6.3 Output Duty Cycle Adjustment

The duty cycle of the output clock can be modified using the OCxDC.OCDC register field. This behavior is only available when MSDIV>0 and LSDIV > 1. When OCDC = 0 the output clock is 50%. Otherwise the clock signal is a pulse with a width of OCDC number of MSDIV output clock periods. The range of OCDC can create pulse widths of 1 to 255 MSDIV output clock periods. When OCxCR2.POL=0, the pulse is high and the signal is low the remainder of the cycle. When POL=1, the pulse is low and the signal is high the remainder of the cycle.

Note that duty cycle adjustment is done in the low-speed divider. Therefore when OCxCR3.LSSEL=0 the duty cycle of the output is not affected. Also, when a CMOS output is configured with OCxCR3.LSSEL=0 and OCxCR3.NEGLSD=1, the OCxN pin has duty cycle adjustment but the OCxP pin does not. This allows a higher-speed 50% duty cycle clock signal to be output on the OCxP pin and a lower-speed frame/phase/time pulse (e.g. 2kHz, 8kHz or 1PPS) to be output on the OCxN pin at the same time.

An output configured for CMOS or HSTL signal format should not be configured to have a duty cycle with high time shorter than 2ns or low time shorter than 2ns.

4.6.4 Output Phase Adjustment

The phase of an output signal can be shifted by 180° by setting OCxCR2.POL=1. In addition, the phase can be adjusted using the OCxPH.PHADJ register field. The adjustment is in units of bank source clock cycles. For example, if the bank source clock is 625MHz then one bank source clock cycle is 1.6ns, the smallest phase adjustment is 0.8ns, and the adjustment range is ±5.6ns.

4.6.5 Output-to-Output Phase Alignment

A 0-to-1 transition of the P1CR1.DALIGN bit causes a simultaneous reset of the medium-speed dividers and low-speed dividers for all output clocks following Path 1 where OCxCR1.PHEN=1. After this reset, all PHEN=1 output clocks with frequencies that are exactly integer multiples of one another are rising-edge aligned, with the phase of each output clock signal adjusted as specified by its OCxPH.PHADJ register field. Similarly a 0-to-1 transition of the P2CR1.DALIGN bit aligns all output clocks following Path 2 where OCxCR1.PHEN=1. Alignment is not glitchess; i.e. it may cause a short high time or low time on participating output clock signals. A glitchless alignment can be accomplished by first stopping the clocks, then aligning them, then starting them. Output clock start and stop is described in section 4.6.6.

4.6.6 Output Clock Start and Stop

Output clocks can be stopped high or low or high-impedance. One use for this behavior is to ensure “glitchless” output clock operation while the output is reconfigured or phase aligned with some other signal.

Each output has an OCxSTOP register with fields to control this behavior. The OCxSTOP.MODE field specifies whether the output clock signal stops high, low, or high-impedance. The OCxSTOP.SRC field specifies the source of the stop signal. Options include control bits or one of the GPIO pins. When OCxSTOP.SRC=0001 the output clock is stopped when the corresponding bit is set in the STOPCR registers OR the MCR1.STOP bit is set.

When the stop mode is Stop High (OCxSTOP.MODE=x1) and the stop signal is asserted, the output clock is stopped after the next rising edge of the output clock. When the stop mode is Stop Low (OCxSTOP.MODE=x0) and the stop signal is asserted, the output clock is stopped after the next falling edge of the output clock. When the output is stopped, the output driver can optionally go high-impedance (OCxSTOP.MODE=1x). Internally the clock signal continues to toggle while the output is stopped. When the stop signal is deasserted, the output clock resumes on the opposite edge that it stopped on. Low-speed output clocks can take long intervals before being stopped after the stop signal goes active. For example, a 1 Hz output could take up to 1 second to stop.

When OCxCR2.POL=1 the output stops on the opposite polarity that is specified by the OCxSTOP.MODE field.

Generally OCxCR1.MSDIV must be > 0 for this function to operate correctly since MSDIV=0 bypasses the start-stop circuits.

When MSDIV=0, OCxSTOP.MODE=11 (stop high then go high-impedance) can be used to make outputs high-impedance, but the action won’t necessarily be glitchless. To use this behavior to get “stop *low* then go-impedance” behavior, OCxCR2.POL can be set to 1.

Note that when OCxCR3.NEGLSD=1 the start-stop logic is bypassed for the OCxN pin, and OCxN may not start/stop without glitches.

Each output has a status register (OCxSR) with several stop/start status bits. The STOPD bit is a real-time status bit indicating stopped or not stopped. The STOPL bit is a latched status bit that is set when the output clock has stopped. The STARTL bit is a latched status bit that is set when the output clock has started.

4.7 Microprocessor Interface

The device can communicate over a SPI interface or an I^2C interface.

In SPI mode ZL4025x devices without internal EEPROM can be configured at reset to be a SPI slave to a processor master or a SPI master to an external EEPROM slave. (SPI master operation changes to SPI slave operation after auto-configuration from the external EEPROM is complete.) The ZL4025x devices with internal EEPROM can only be configured as a SPI slave to a processor master. All devices are always slaves on the I^2C bus.

Section 4.2 describes reset pin settings required to configure the device for these interfaces.

4.7.1 SPI Slave

The device can present a SPI slave port on the CSN, SCLK, MOSI, and MISO pins. SPI is a widely used master/slave bus protocol that allows a master and one or more slaves to communicate over a serial bus. SPI masters are typically microprocessors, ASICs or FPGAs. Data transfers are always initiated by the master, which also generates the SCLK signal. The device receives serial data on the MOSI (Master Out Slave In) pin and transmits serial data on the MISO (Master In Slave Out) pin. MISO is high impedance except when the device is transmitting data to the bus master.

Bit Order. The register address and all data bytes are transmitted most significant bit first on both MOSI and MISO.

Clock Polarity and Phase. The device latches data on MOSI on the rising edge of SCLK and updates data on MISO on the falling edge of SCLK. SCLK does not have to toggle between accesses, i.e., when CSN is high.

Device Selection. Each SPI device has its own chip-select line. To select the device, the bus master drives its CSN pin low.

Command and Address. After driving CSN low, the bus master transmits an 8-bit command followed by a 16-bit register address. The available commands are shown below.

Table 3 - SPI Commands

Command	Hex	Bit Order, Left to Right
Write Enable	0x06	0000 0110
Write	0x02	0000 0010
Read	0x03	0000 0011
Read Status	0x05	0000 0101

Read Transactions. The device registers are accessible when EESEL=0. On ZL4025x devices with internal EEPROM, the EEPROM memory is accessible when the EESEL bit is 1. On ZL4025x devices without internal EEROM, the EESEL bit must be set to 0. After driving CSN low, the bus master transmits the read command followed by the 16-bit address. The device then responds with the requested data byte on MISO, increments its address counter, and prefetches the next data byte. If the bus master continues to demand data, the device continues to provide the data on MISO, increment its address counter, and prefetch the following byte. The read transaction is completed when the bus master drives CSN high. See Figure 5.

Register Write Transactions. The device registers are accessible when EESEL=0. After driving CSN low, the bus master transmits the write command followed by the 16-bit register address followed by the first data byte to be written. The device receives the first data byte on MOSI, writes it to the specified register, increments its internal address register, and prepares to receive the next data byte. If the master continues to transmit, the device continues to write the data received and increment its address counter. The write transaction is completed when the bus master drives CSN high. See Figure 7.

EEPROM Writes (ZL40251, ZL40253 Only). The internal EEPROM memory is accessible when the EESEL bit is 1. After driving CSN low, the bus master transmits the write enable command and then drives CSN high to set the internal write enable latch. The bus master then drives CSN low again and transmits the write command followed by the 16-bit address followed by the first data byte to be written. The device first copies the page to be written from EEPROM to its page buffer. The device then receives the first data byte on MOSI, writes it to its page buffer,

increments its internal address register, and prepares to receive the next data byte. If the master continues to transmit, the device continues to write the data received to its page buffer and continues to increment its address counter. The address counter rolls over at the 32-byte page boundary (i.e. when the five least-significant address bits are 11111). When the bus master drives CSN high, the device transfers the data in the page buffer to the appropriate page in the EEPROM memory. See Figure 6 and Figure 7.

EEPROM Read Status (ZL40251, ZL40253 Only). After the bus master drives CSN high to end an EEPROM write command, the EEPROM memory is not accessible for up to 5ms while the data is transferred from the page buffer. To determine when this transfer is complete, the bus master can use the Read Status command. After driving CSN low, the bus master transmits the Read Status command. The device then responds with the status byte on MISO. In this byte, the least significant bit is set to 1 if the transfer is still in progress and 0 if the transfer has completed.

Early Termination of Bus Transactions. The bus master can terminate SPI bus transactions at any time by pulling CSN high. In response to early terminations, the device resets its SPI interface logic and waits for the start of the next transaction. If a register write transaction is terminated prior to the SCLK edge that latches the least significant bit of a data byte, the data byte is not written. On devices with internal EEPROM, if an EEPROM write transaction is terminated prior to the SCLK edge that latches the least significant bit of a data byte, none of the bytes in that write transaction are written.

Design Option: Wiring MOSI and MISO Together. Because communication between the bus master and the device is half-duplex, the MOSI and MISO pins can be wired together externally to reduce wire count. To support this option, the bus master must not drive the MOSI/MISO line when the device is transmitting.

AC Timing. See Table 15 and Figure 17 for AC timing specifications for the SPI interface.

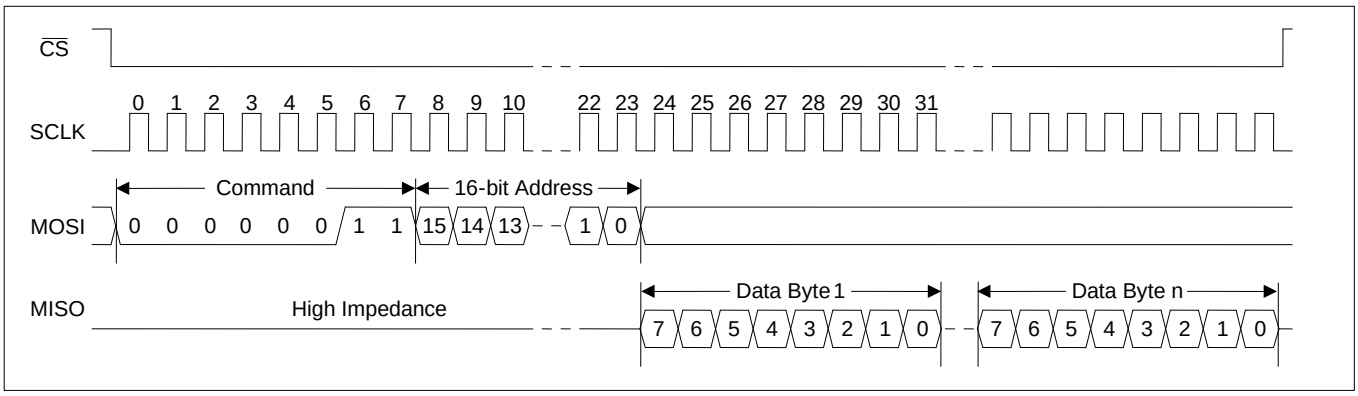


Figure 5 - SPI Read Transaction Functional Timing

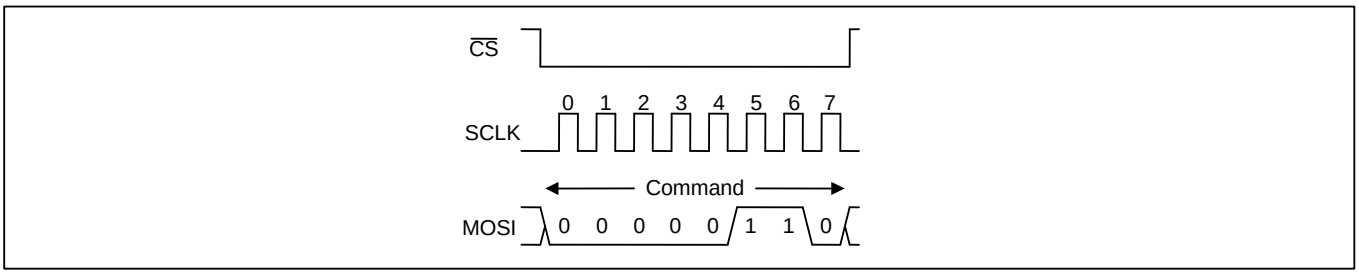


Figure 6 - SPI Write Enable Transaction Functional Timing (ZL40251 and ZL40253 Only)

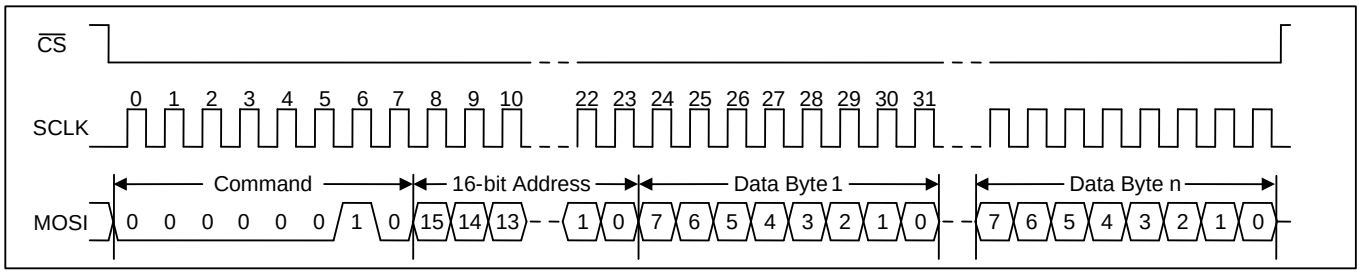


Figure 7 - SPI Write Transaction Functional Timing

4.7.2 SPI Master (ZL40250 and ZL40252 Only)

After reset these devices can present a SPI master port on the CSN, SCLK, MOSI, and MISO pins for auto-configuration using data read from an external SPI EEPROM. During auto-configuration the device is always the SPI master and generates the CSN and SCLK signals. The device transmits serial data on the the MOSI (Master Out Slave In) pin and receives serial data on the MISO (Master In Slave Out) pin.

Bit Order. The register address and all data bytes are transmitted most significant bit first on both MOSI and MISO.

Clock Polarity and Phase. The device latches data on MISO on the rising edge of SCLK and updates data on MOSI on the falling edge of SCLK.

Device Selection. Each SPI device has its own chip-select line. To select the external EEPROM, the device drives the CSN signal low.

Command and Address. After driving CSN low, the device transmits an 8-bit read command followed by a 16-bit register address. The read command is shown below.

Command	Hex	Bit Order, Left to Right
Read	0x03	0000 0011

Read Transactions. After driving CSN low, the device transmits the read command followed by the 16-bit register address. The external EEPROM then responds with the requested data byte on MISO, increments its address counter, and prefetches the next data byte. If the device continues to demand data, the EEPROM continues to provide the data on MISO, increment its address counter, and prefetch the following byte. The read transaction is completed when the device drives CSN high. See Figure 5.

Writing the External EEPROM. Due to the small package size and low pin count of the device, there is no way to use the ZL40250 or ZL40252 to write the external EEPROM. The auto-configuration data used by the ZL40250 or ZL40252 must be pre-programmed into the EEPROM by some other method, such as:

1. The EEPROM manufacturer can write the data to the EEPROM during production testing. This is a service they routinely provide.
2. A contract manufacturer or distributor can write the data to the EEPROM using a production EEPROM programmer before the EEPROM is mounted to the board.

4.7.3 I²C Slave

The device can present a fast-mode (400kbit/s) I²C slave port on the SCL and SDA pins. I²C is a widely used master/slave bus protocol that allows one or more masters and one or more slaves to communicate over a two-wire serial bus. I²C masters are typically microprocessors, ASICs or FPGAs. Data transfers are always initiated by the master, which also generates the SCL signal. The device is compliant with version 2.1 of the I²C specification.

The I²C interface on the device is a protocol translator from external I²C transactions to internal SPI transactions. This explains the slightly increased protocol complexity described in the paragraphs that follow.

Read Transactions. The device registers are accessible when the EESEL bit is 0. On ZL40251 and ZL40253 the internal EEPROM memory is accessible when the EESEL bit is 1. On ZL40250 and ZL40252 the EESEL bit must be set to 0. The bus master first does an I²C write to the device. In this transaction three bytes are written: the SPI Read command (see Table 3), the upper byte of the register address, and the lower byte of the register address. The bus master then does an I²C read. During each acknowledge (A) bit the device fetches data from the read address and then increments the read address. The device then transmits the data to the bus master during the next 8 SCL cycles. The bus master terminates the read with a not-acknowledge (NA) followed by a STOP condition (P). See Figure 8. After the I²C write there can be unlimited idle time on the bus before the I²C read, but the device cannot tolerate other I²C bus traffic between the I²C write and the I²C read. Care must be taken to ensure that the I²C read is the first command on the bus after the I²C write to ensure the two-part read transaction happens correctly.

Register Write Transactions. The device registers are accessible when the EESEL bit is 0. The bus master does an I²C write to the device. The first three bytes of this transaction are the SPI Write command (see Table 3), the upper byte of the register address, and the lower byte of the register address. Subsequent bytes are data bytes to be written. After each data byte is received, the device writes the byte to the write address and then increments the write address. The bus master terminates the write with a STOP condition (P). See Figure 9.

EEPROM Writes (ZL40251 and ZL40253 Only). The EEPROM memory is accessible when the EESEL bit is 1. The bus master first does an I²C write to transmit the SPI Write Enable command (see Table 3) to the device. The bus master then does an I²C write to transmit data to the device as described in the Register Write Transactions paragraph above. See Figure 10.

EEPROM Read Status (ZL40251 and ZL40253 Only). The bus master first does an I²C write to transmit the SPI Read Status command (see Table 3) to the device. The bus master then does an I²C read to get the status byte. In this byte, the least significant bit is set to 1 if the transfer is still in progress and 0 if the transfer has completed. See Figure 11. Similar to read transactions described above, the I²C write and the I²C read cannot be separated by other I²C bus traffic.

I²C Features Not Supported by the Device. The I²C specification has several optional features that are not supported by the device. These are: 3.4Mbit/s high-speed mode (Hs-mode), 10-bit device addressing, general call address, software reset, and device ID. The device does not hold SCL low to force the master to wait.

I²C Slave Address. By default the upper 5 bits of the device's 7-bit slave address are fixed at 11101 and the lower 2 bits can be pin-configured for any of three values as shown in the table in section 4.2. For a device that can auto-configure from EEPROM at power-up, its I²C slave address can be set to any value during auto-configuration at power-up by writing the the I2CA register as part of the configuration script.

Bit Order. The I²C specification requires device address, register address and all data bytes to be transmitted most significant bit first on the SDA signal.

Note: as required by the I²C specification, when power is removed from the device, the SDA and SCL pins are left floating so they don't obstruct the bus lines.

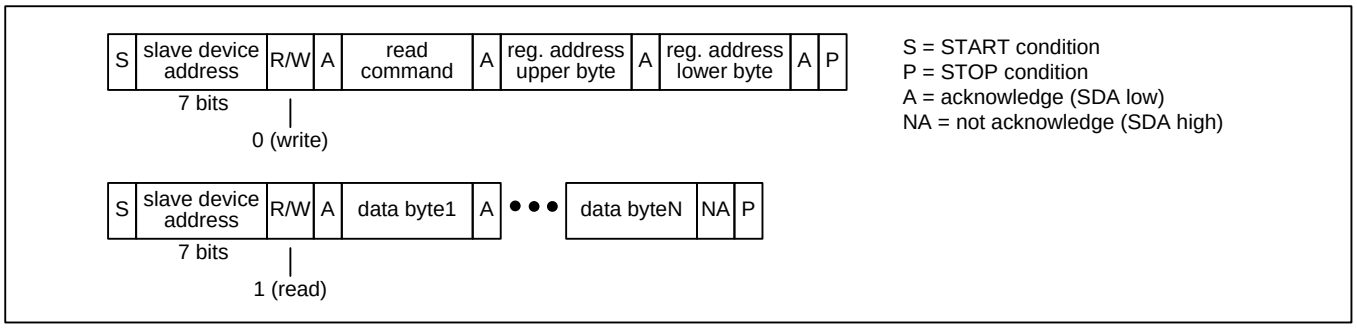


Figure 8 - I²C Read Transaction Functional Timing

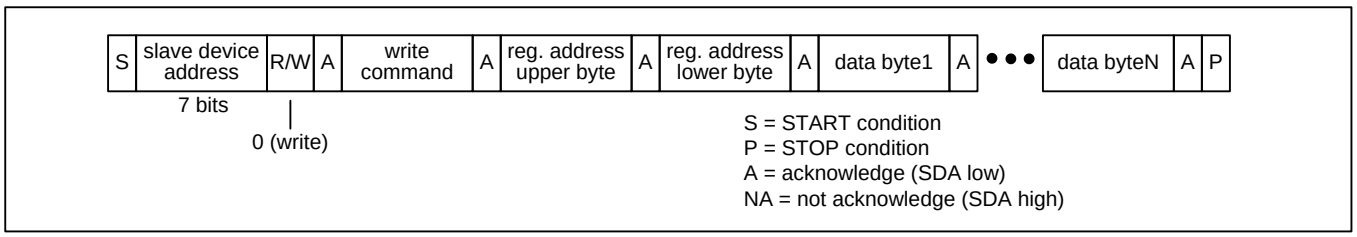


Figure 9 - I²C Register Write Transaction Functional Timing

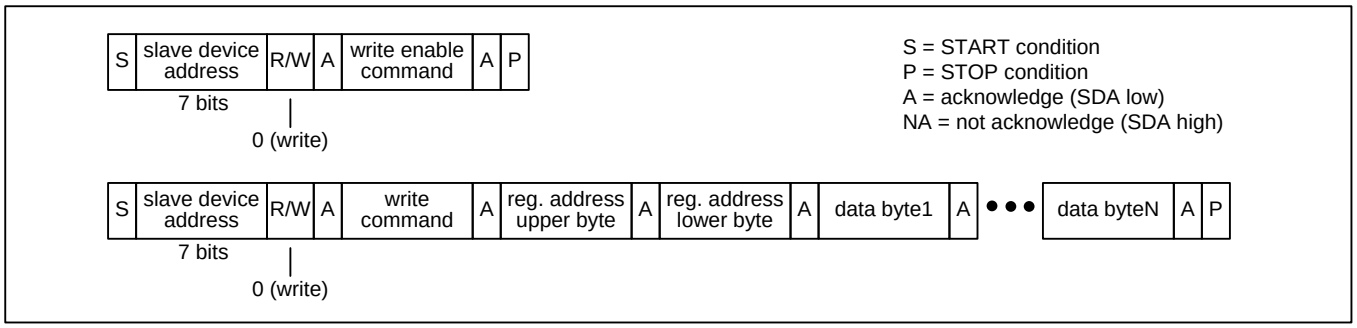


Figure 10 - I²C EEPROM Write Transaction Functional Timing (ZL40251 and ZL40253 Only)

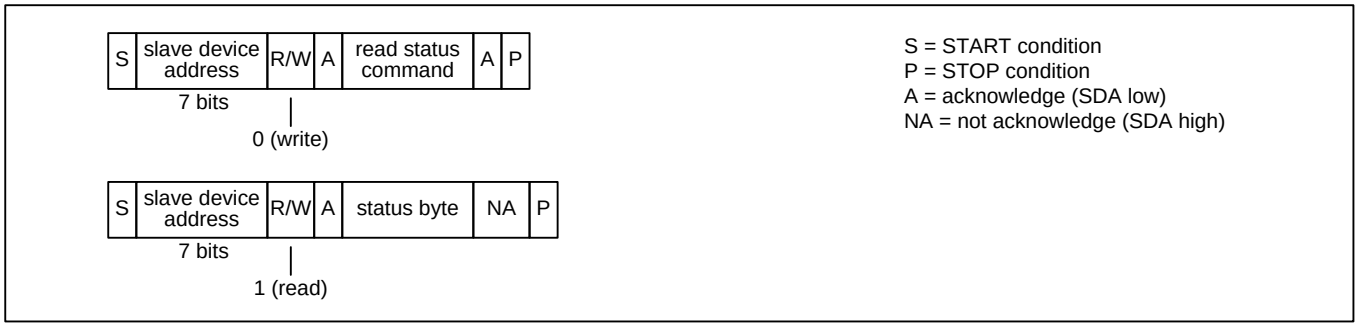


Figure 11 - I²C EEPROM Read Status Transaction Functional Timing (ZL40251 and ZL40253 Only)

Note: In Figure 8 through Figure 11, a STOP condition (P) immediately followed by a START condition (S) can be replaced by a repeated START condition (Sr) as described in the I²C specification.

4.8 Interrupt Logic

Any of the GPIO pins can be configured as an interrupt-request output by setting the appropriate GPIOxC field in the GPIOCR registers to one of the status output options (01xx) and configuring the appropriate GPIOxSS register to follow the INTSR.INT bit. If system software is written to poll rather than receive interrupt requests, then software can read the INTSR.INT bit first to determine if any interrupt requests are active in the device.

Many of the latched status bits in the device can be the source of an interrupt request if their corresponding interrupt enable bits are set. The device's interrupt logic is shown in Figure 12. See the register map (Table 4) and the status register descriptions in section 5.3.2 for descriptions of the register bits shown in the figure.

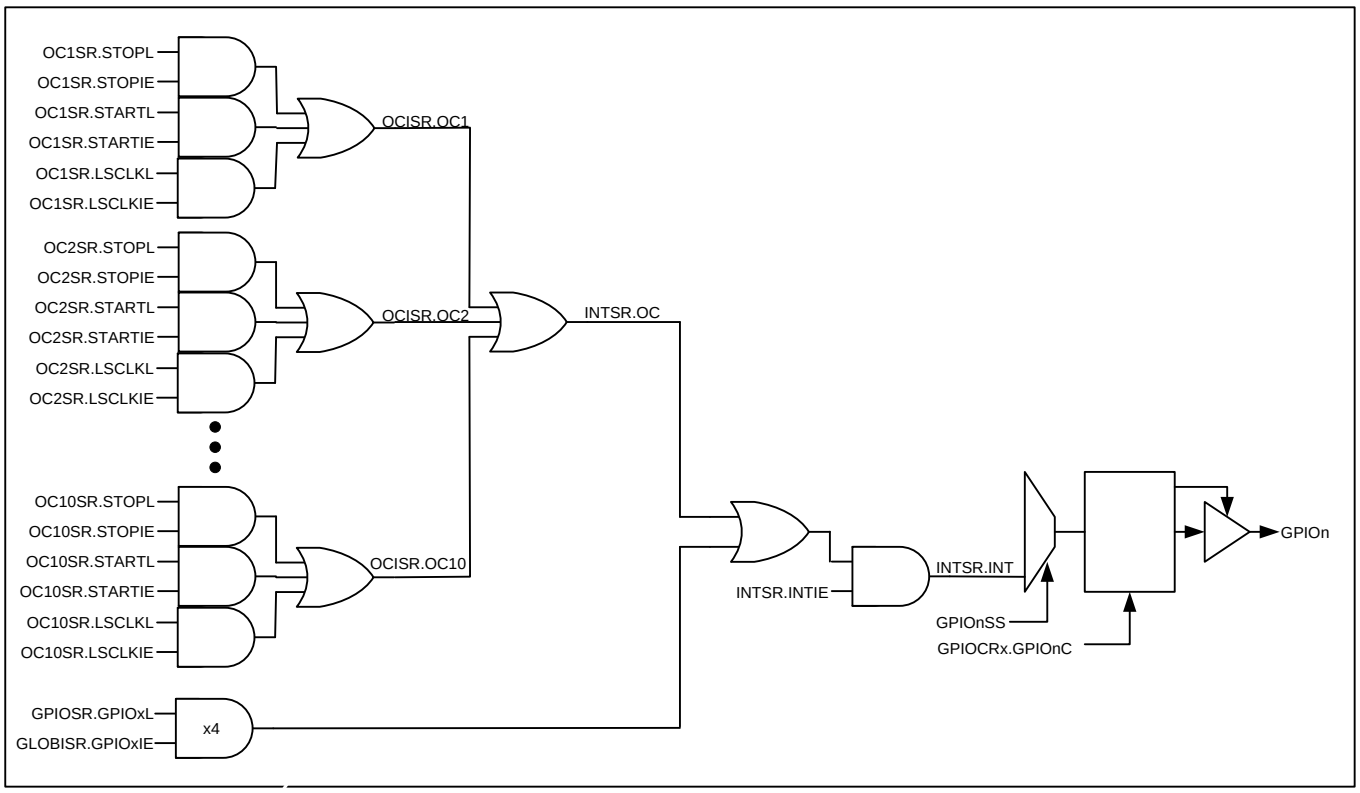


Figure 12 - Interrupt Structure

4.9 Reset Logic

The device has three reset controls: the RSTN pin, and the hard reset (HRST) and soft reset (SRST) bits in MCR1. The RSTN pin asynchronously resets the entire device. When the RSTN pin is low all internal registers are reset to their default values. When RSTN returns high the device's auto-configuration boot controller is started. **The RSTN pin must be asserted once after power-up.** Reset should be asserted for at least 1µs. See section 4.9.1 below for important details about using an external RC reset circuit with the RSTN pin.

Asserting the MCR1.HRST (hard reset) bit is functionally similar to asserting the RSTN pin. The HRST bit resets the entire device except for the microprocessor interface, the HRST bit itself, the I2CA register, and CFGSR.IF[1:0]. While HRST=1 the device accepts register writes so that HRST can be set back to 0, but register reads are not allowed. When HRST is set back to 0, the TEST and AC[2:0] pins are sampled as described in section 4.2, but, unlike when RSTN is deasserted, the IF[1:0] pins are not sampled so that the device remains in the same interface mode (SPI or I^2C) and maintains the same slave address when in I^2C mode. When HRST is set back to 0, the device's auto-configuration boot controller is started after a 1 to 3µs delay.

The MCR1.SRST (soft reset) bit resets the entire device except for the microprocessor interface, the SRST bit itself, the MCR1.HRST bit, the I2CA register, and the CFGSR register. When the SRST bit is asserted the device's auto-configuration boot controller is **not** started.

Microsemi recommends holding RSTN low while the internal ring oscillator starts up and stabilizes. An incorrect reset condition could result if RSTN is released before the oscillator has started up completely.

Important: System software must wait at least 100µs after RSTN is deasserted and wait for GLOBISR.BCDONE=1 before configuring the device.

4.9.1 Design Considerations for Using an External RC Reset Circuit

When the power supply arrangement for the device has VDDH=VDDL (3.3V or 2.5V) an external RC reset circuit can be used to reset the device during power-up with no additional considerations.

When the power supply arrangement for the device has VDDL=1.8V then the board designer should choose one of two options: (a) a power-on-reset (POR) chip such as a Texas Instruments TPS3839 should be used instead of an external RC reset circuit, or (b) the device's VDDIO pin must be wired to VDDL. In option (a) during the interval between VDDH ramping and VDDL ramping the RSTN pin can briefly behave as an output driving high. Therefore a current-limiting series resistor should be used between the POR chip and the device RSTN pin.

The possible disadvantage of option (b) is that VDDIO, the power supply for all SPI/I2C pins and all GPIO pins, could be too low if neighboring devices operate at power supply voltages higher than VDDL. One exception to this disadvantage would be the I2C interface. Since I2C's logic-high voltage is set by pull-up resistors, those resistors can be externally wired to a voltage higher than VDDIO up to 3.3V. The SCL/SCLK and SDA/MOSI pins are 3.3V tolerant.

4.10 Power-Supply Considerations

Due to the multi-power-supply nature of the device, some I/Os have parasitic diodes between a lower-voltage supply and a higher-voltage supply. When ramping power supplies up or down, care must be taken to avoid forward-biasing these diodes because it could cause latchup. Two methods are available to prevent this. The first method is to place a Schottky diode external to the device between the lower-voltage supply and the higher-voltage supply to force the higher-voltage supply to be within one parasitic diode drop of the lower-voltage supply. The second method is to ramp up the higher-voltage supply first and then ramp up the lower-voltge supply.

Important Note: The voltages on VDDL, VDDIO, and all VDDOx pins must not exceed VDDH. Not complying with this requirement may damage the device.

4.11 Auto-Configuration from EEPROM or ROM

For ZL40250 and ZL40252, the device optionally can configure itself at reset from an internal ROM. The ROM stores eight configurations, known as configurations 0 through 7. As described in section 4.2.1, IF[1:0] must be 00, 01 or 10 at reset, and the device configuration to be used is specified by the values of the AC[2:0] pins at reset (0 through 7). Descriptions of the standard-product ROM configurations are available from Microsemi.

For ZL40250 and ZL40252, the device optionally can configure itself at reset from an external EEPROM connected to its SPI interface. The EEPROM can store up to eight configurations, known as configurations 0 through 7. As described in section 4.2.1, IF[1:0] must be 11 at reset, and the device configuration to be used is specified by the values of the AC[2:0] pins at reset (0 through 7).

For ZL40251 and ZL40253, the internal EEPROM memory can store up to eight device configurations, known as configurations 0 through 7. As described in section 4.2.2, the device configuration to be used is specified by the values of the AC[2:0] pins at reset.

4.11.1 Generating Device Configurations

Device configurations are most easily generated using the evaluation software. This is true for auto-configurations stored in internal or external EEPROM and for configurations that are written to the device by a system processor. See section 4.12 for guidance if device configurations must be developed without using the evaluation software.

4.11.2 Direct EEPROM Write Mode (ZL40251 and ZL40253 Only)

To simplify writing the device's internal EEPROM during manufacturing, the device has a test mode known as direct EEPROM write mode. The device enters this mode when TEST=1, AC[2:0]=000 and IF[1:0]=11 on the rising edge of RSTN. In this mode the EEPROM memory is mapped into the address map and can be written as needed to store configuration scripts in the device. Device registers are not accessible in this mode. The device exits this mode on the rising edge of RSTN. Note: the device drives the MISO pin continually during this mode. Therefore this mode cannot be used when MOSI and MISO are tied together as described in the **Design Option: Wiring MOSI and MISO Together** paragraph in section 4.7.1.

4.11.3 Holding Other Devices in Reset During Auto-Configuration

Using the appropriate GPIOCR and GPIO0SS registers, a GPIO pin can be configured to follow the GLOBISR.BCDONE status bit. This GPIO can then be used as a reset signal to hold other devices (device that use clocks from this device) in reset while the device configures itself. As an example, to configure GPIO0 to follow BCDONE with 0=reset add the following writes at the beginning of the configuration file: write 0x1F to GPIO0SS and write 0x04 to GPIOCR1.

4.12 Configuration Sequence

Device configurations are most easily generated using the evaluation software, which automatically generates configurations that follow Microsemi's suggested sequence. To develop device configurations manually (i.e. from device documentation rather than the evaluation software) see Application Note ZLAN-591 for Microsemi's suggested device configuration sequence.

4.13 Power Supply Decoupling and Layout Recommendations

Application Note ZLAN-592 describes recommended power supply decoupling and layout practices.

5. Register Descriptions

Table 4 shows the register map. In each register, bit 7 is the MSb and bit 0 is the LSb. Register addresses not listed are reserved. Bits marked "—" are reserved and must be written with 0. Writing other values to these registers may put the device in a factory test mode resulting in undefined operation. Bits labeled "0" or "1" must be written with that value for proper operation. Register fields with underlined names are read-only fields; writes to these fields have no effect. All other fields are read-write. Register fields are described in detail in the register descriptions that follow Table 4.

5.1 Register Types

5.1.1 Status Bits

The device has two types of status bits. Real-time status bits are read-only and indicate the state of a signal at the time it is read. Latched status bits are set when a signal changes state (low-to-high, high-to-low, or both, depending on the bit) and cleared when written with a logic 1 value. Writing a 0 has no effect. When set, some latched status

bits can cause an interrupt request if enabled to do so by corresponding interrupt enable bits. Status bits marked "—" are reserved and must be ignored.

5.1.2 Configuration Fields

Configuration fields are read-write. During reset, each configuration field reverts to the default value shown in the register definition. Configuration register bits marked "—" are reserved and must be written with 0.

5.1.3 Bank-Switched Registers (ZL40251 and ZL40253 Only)

The EESEL register is a bank-select control field that maps the device registers into the memory map at address 0x1 and above when the EESEL bit is 0 and maps the EEPROM memory into the memory map at address 0x1 and above when the EESEL bit is 1. The EESEL register itself is always in the memory map at address 0x0.

5.2 Register Map

Table 4 - Register Map

ADDR	REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Global Configuration Registers									
00h	EESEL	EESEL	—	—	—	—	—	—	—
01	MCR1	SRST	HRST	STOP	—	ROSCD	AINCDIS	ODMISO	—
02	MCR2	—	—	—	—	—	—	XAB[1:0]	
04	ICEN	—	—	—	—	—	IC3EN	IC2EN	IC1EN
05	OCEN1	OC8EN	OC7EN	OC6EN	OC5EN	OC4EN	OC3EN	OC2EN	OC1EN
06	OCEN2	—	—	—	—	—	—	OC10EN	OC9EN
07	OCMUX1	—	—	OCMUXC[1:0]		OCMUXB[1:0]		OCMUXA[1:0]	
08	OCMUX2	—	—	OCMUXF[1:0]		OCMUXE[1:0]		OCMUXD[1:0]	
09	STOPCR1	OC8	OC7	OC6	OC5	OC4	OC3	OC2	OC1
0A	STOPCR2	—	—	—	—	—	—	OC10	OC9
0B	GPIOCR1	GPIO1C[3:0]				GPIO0C[3:0]			
0C	GPIOCR2	GPIO3C[3:0]				GPIO2C[3:0]			
0D	GPIO0SS	REG[4:0]					BIT[2:0]		
0E	GPIO1SS	REG[4:0]					BIT[2:0]		
0F	GPIO2SS	REG[4:0]					BIT[2:0]		
10	GPIO3SS	REG[4:0]					BIT[2:0]		
11	I2CA	—	I2CA[6:0]						
Status Registers									
30	ID1	IDU[7:0]							
31	ID2	IDL[3:0]				REV[3:0]			
40	CFGSR	CFGD	—	IF[1:0]		TEST	AC[2:0]		
41	GPIOSR	GPIO3L	GPIO2L	GPIO1L	GPIO0L	GPIO3	GPIO2	GPIO1	GPIO0
42	INTSR	—	—	OC	—	—	—	INTIE	INT
43	GLOBISR	BCDONE	—	—	—	GPIO3IE	GPIO2IE	GPIO1IE	GPIO0IE
45	OCISR1	OC8	OC7	OC6	OC5	OC4	OC3	OC2	OC1
46	OCISR2	—	—	—	—	—	—	OC10	OC9
48	P1SR	—	—	—	—	—	—	—	SELREF
49	P2SR	—	—	—	—	—	—	—	SELREF
50	OC1SR	LSCLKIE	LSCLKL	LSCLK	STARTIE	STARTL	STOPIE	STOPL	STOPD
51	OC2SR	LSCLKIE	LSCLKL	LSCLK	STARTIE	STARTL	STOPIE	STOPL	STOPD
52	OC3SR	LSCLKIE	LSCLKL	LSCLK	STARTIE	STARTL	STOPIE	STOPL	STOPD
53	OC4SR	LSCLKIE	LSCLKL	LSCLK	STARTIE	STARTL	STOPIE	STOPL	STOPD
54	OC5SR	LSCLKIE	LSCLKL	LSCLK	STARTIE	STARTL	STOPIE	STOPL	STOPD
55	OC6SR	LSCLKIE	LSCLKL	LSCLK	STARTIE	STARTL	STOPIE	STOPL	STOPD
56	OC7SR	LSCLKIE	LSCLKL	LSCLK	STARTIE	STARTL	STOPIE	STOPL	STOPD
57	OC8SR	LSCLKIE	LSCLKL	LSCLK	STARTIE	STARTL	STOPIE	STOPL	STOPD
58	OC9SR	LSCLKIE	LSCLKL	LSCLK	STARTIE	STARTL	STOPIE	STOPL	STOPD
59	OC10SR	LSCLKIE	LSCLKL	LSCLK	STARTIE	STARTL	STOPIE	STOPL	STOPD
Path 1 Configuration Registers									
100	P1CR1	—	DALIGN	EXTSS[1:0]		—	—	1	—
102	P1CR3	—	EXTSW	ALTMUX[2:0]			MUX[2:0]		
Path 2 Configuration Registers									
180	P2CR1	—	DALIGN	EXTSS[1:0]		—	—	1	—
182	P2CR3	—	EXTSW	ALTMUX[2:0]			MUX[2:0]		

ADDR	REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Output Clock Configuration Registers									
	OC1 Registers								
200	OC1CR1	PHEN	MSDIV[6:0]						
201	OC1CR2	—	POL	DRIVE[1:0]		OCSF[3:0]			
202	OC1DIFF	VCM[3:0]				VOD[3:0]			
203	OC1REG	—	—	—	—	VREG[3:0]			
204	OC1CR3	SRLSEN	—	NEGLSD	LSSEL	—	—	—	LSDIV[24]
205	OC1DIV1	LSDIV[7:0]							
206	OC1DIV2	LSDIV[15:8]							
207	OC1DIV3	LSDIV[23:16]							
208	OC1DC	OCDC[7:0]							
209	OC1PH	—	—	—	—	PHADJ[3:0]			
20A	OC1STOP	—	SRC[3:0]				NEGLSD	MODE[1:0]	
	OC2 Registers								
210	OC2CR1	same as OC1 registers							
…	…								
21A	OC2STOP								
	OC3 Registers								
220	OC3CR1	same as OC1 registers							
…	…								
22A	OC3STOP								
	OC4 Registers								
230	OC4CR1	same as OC1 registers							
…	…								
23A	OC4STOP								
	OC5 Registers								
240	OC5CR1	same as OC1 registers							
…	…								
24A	OC5STOP								
	OC6 Registers								
250	OC6CR1	same as OC1 registers							
…	…								
25A	OC6STOP								
	OC7 Registers								
260	OC7CR1	same as OC1 registers							
…	…								
26A	OC7STOP								
	OC8 Registers								
270	OC8CR1	same as OC1 registers							
…	…								
27A	OC8STOP								
	OC9 Registers								
280	OC9CR1	same as OC1 registers							
…	…								
28A	OC9STOP								

ADDR	REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	OC10 Registers								
290	OC10CR1	same as OC1 registers							
…	…								
29A	OC10STOP								
Input Clock Configuration									
300	XACR1	—	POL	—	—	—	—	HSDIV[1:0]	
301	XACR2	XOAMP[7:0]							
302	XACR3	XBCAP[3:0]				XACAP[3:0]			
303	IC1CR1	—	POL	—	—	—	—	HSDIV[1:0]	
304	IC2CR1	—	POL	—	—	—	—	HSDIV[1:0]	
305	IC3CR1	—	POL	—	—	—	—	HSDIV[1:0]	

5.3 Register Definitions

5.3.1 Global Configuration Registers

Register Name: EESEL
Register Description: EEPROM Memory Selection Register
Register Address: 00h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	EESEL	—	—	—	—	—	—	—
Default	0	0	0	0	0	0	0	0

Bit 7: EEPROM Memory Select (EESEL). This bit is a bank-select that specfies whether device register space or EEPROM memory is mapped into addresses 0x1 and above. This applies only to the ZL40251 and ZL40253. The ZL40250 and ZL40252 do not have internal EEPROM memory. Note that ROMSEL has priority over EESEL. See sections 4.7 and 5.1.3.

0 = Device registers
1= EEPROM memory

Register Name: MCR1
Register Description: Master Configuration Register 1
Register Address: 01h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	SRST	HRST	STOP	—	ROSCD	AINCDIS	ODMISO	—
Default	0	0	0	0	0	0	0	0

Bit 7: Soft Reset (SRST). This bit resets the entire device except for the microprocessor interface, the SRST bit itself, the MCR1.HRST bit, the I2CA register, and CFGSR bits 5:0. When SRST is active, the register fields with pin-programmed defaults do not latch their values from the corresponding input pins. When the SRST bit is asserted the device's auto-configuration boot controller is **not** started. See section 4.9.

0 = Normal operation
1 = Reset

Bit 6: Hard Reset (HRST). Asserting this bit is functionally equivalent to asserting the RSTN pin. The HRST bit resets the entire device except for the microprocessor interface and the HRST bit itself. Register fields with pin-programmed defaults latch their values from the corresponding input pins, and the device's auto-configuration boot controller is started. See section 4.9.

0 = Normal operation
1 = Reset

Bit 5: Output Clock Stop (STOP). Asserting this bit stops all output clocks that are configured with OCxSTOP.SRC=0001. Note that this signal is ORed with the per-output stop control bit in the STOPCR registers to make each output's internal stop control signal. See section 4.6.6.

Bit 3: Ring Oscillator Disable (ROSCD). This bit disables the ring oscillator. It can be set to 1 when auto-configuration is complete. See section 4.3.3.

0 = Enable
1 = Disable (power-down)

Bit 1: Open Drain MISO Enable (ODMISO). This bit configures the MISO pin to be open-drain. When this bit is set, the MISO pin only drives low and must have an external pullup resistor.

0 = Disable (MISO drives 0 and 1, high-impedance when not driven)
1 = Enable (MISO drives 0 only, high-impedance all other times)

Register Name: MCR2
Register Description: Master Configuration Register 2
Register Address: 02h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	—	—	—	—	—	XAB[1:0]	
Default	0	0	0	0	0	0	0	0

Bits 1 to 0: XA/XB Pin Mode (XAB[1:0]). This field specifies the behavior of the XA and XB pins. See section 4.3.

00 = Crystal driver and input disabled / powered down
01 = Crystal driver and input enabled on XA/XB
10 = XA enabled as single-ended input for external oscillator signal; XB must be left floating
11 = {unused value}

Register Name: ICEN
Register Description: Input Clock Enable Register
Register Address: 04h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	—	—	—	—	IC3EN	IC2EN	IC1EN
Default	0	0	0	0	0	0	0	0

Bit 2: Input Clock 3 Enable (IC3EN). This bit enables and disables the input clock 3 differential receiver and input dividers. See section 4.4.
0 = Disabled
1 = Enabled

Bit 1: Input Clock 2 Enable (IC2EN). This bit enables and disables the input clock 2 differential receiver and input dividers. See section 4.4.
0 = Disabled
1 = Enabled

Bit 0: Input Clock 1 Enable (IC1EN). This bit enables and disables the input clock 1 differential receiver and input dividers. See section 4.4.
0 = Disabled
1 = Enabled

Register Name: OCEN1
Register Description: Output Clock Enable Register 1
Register Address: 05h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	OC8EN	OC7EN	OC6EN	OC5EN	OC4EN	OC3EN	OC2EN	OC1EN
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: Output Clock x Enable (OCxEN). Each of these bits enables and disables the corresponding output dividers, phase adjustment/alignment circuitry and start/stop circuitry. See section 4.6.1.
0 = Disabled
1 = Enabled

Note: On Rev A devices at least one OCxEN bit must be set for each of the six output banks for proper operation. These bits should be set at or near the beginning of the configuration sequence.

Register Name: OCEN2
Register Description: Output Clock Enable Register 2
Register Address: 06h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	—	—	—	—	—	OC10EN	OC9EN
Default	0	0	0	0	0	0	0	0

See the OCEN1 register description above.

Register Name: OCMUX1
Register Description: Output Clock Mux Register 1
Register Address: 07h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	-	-	OCMUXC		OCMUXB		OCMUXA	
Default	0	0	0	0	0	0	0	0

Bits 5 to 4: Output Clock Mux C (OCMUXC[1:0]). Controls the high speed output mux for output group C (OC4 and OC5).
01 = Path 1 (see block diagram in Figure 1)
11 = Path 2
00, 10 = {unused value}

Bits 3 to 2: Output Clock Mux B (OCMUXB[1:0]). Controls the high speed output mux for output group B (OC3).
01 = Path 1 (see block diagram in Figure 1)
11 = Path 2
00, 10 = {unused value}

Bits 1 to 0: Output Clock Mux A (OCMUXA[1:0]). Controls the high speed output mux for output group A (OC1 and OC2).
01 = Path 1 (see block diagram in Figure 1)
11 = Path 2
00, 10 = {unused value}

Register Name: OCMUX2
Register Description: Output Clock Mux Register 2
Register Address: 08h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	-	-	OCMUXF		OCMUXE		OCMUXD	
Default	0	0	0	0	0	0	0	0

Bits 5 to 4: Output Clock Mux F (OCMUXF[1:0]). Controls the high speed output mux for output group F (OC9 and OC10).
01 = Path 1 (see block diagram in Figure 1)
11 = Path 2
00, 10 = {unused value}

Bits 3 to 2: Output Clock Mux E (OCMUXE[1:0]). Controls the high speed output mux for output group E (OC8).
01 = Path 1 (see block diagram in Figure 1)
11 = Path 2
00, 10 = {unused value}

Bits 1 to 0: Output Clock Mux D (OCMUXD[1:0]). Controls the high speed output mux for output group D (OC6 and OC7).
01 = Path 1 (see block diagram in Figure 1)
11 = Path 2
00, 10 = {unused value}

Register Name: STOPCR1
Register Description: Output Clock Stop Control Register 1
Register Address: 09h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	OC8STP	OC7STP	OC6STP	OC5STP	OC4STP	OC3STP	OC2STP	OC1STP
Default	0	0	0	0	0	0	0	0

Bit 7: OC8 Stop Control (OC8STP). When SRC=0001 in the OC8STOP register, setting this bit to 1 causes OC8 to stop. Note that this signal is ORed with MCR1.STOP to make OC8's internal stop control signal. See section 4.6.6.

Bits 6 to 0: These bits are similar to OC8STP above but for OC7 through OC1.

Register Name: STOPCR2
Register Description: Output Clock Stop Control Register 2
Register Address: 0Ah

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	—	—	—	—	—	OC10STP	OC9STP
Default	0	0	0	0	0	0	0	0

Bits 1 to 0: These bits are similar to STOPCR1.OC8STP but for OC10 and OC9.

Register Name: GPIOCR1
Register Description: GPIO Configuration Register 1
Register Address: 0Bh

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	GPIO1C[3:0]				GPIO0C[3:0]			
Default	0	0	0	0	0	0	0	0

Bits 7 to 4: GPIO1 Configuration (GPIO1C[3:0]). This field configures the GPIO1 pin as a general-purpose input, a general-purpose output driving low or high, or a status output. The current state of the pin can be read from GPIOSR.GPIO1. When GPIO1 is a status output, the GPIO1SS register specifies which status bit is output.

0000 = General-purpose input
0001 = General-purpose input - inverted polarity
0010 = General-purpose output driving low
0011 = General-purpose output driving high
0100 = Status output – non-inverted polarity
0101 = Status output - inverted polarity of the status bit it follows
0110 = Status output – 0 drives low, 1 high impedance
0111 = Status output – 0 high impedance, 1 drives low
1000 to 1111 = {unused values}

Bits 3 to 0: GPIO0 Configuration (GPIO0C[3:0]). This field configures the GPIO0 pin as a general-purpose input, a general-purpose output driving low or high, or a status output. The current state of the pin can be read from GPIOSR.GPIO0. When GPIO0 is a status output, the GPIO0SS register specifies which status bit is output.

0000 = General-purpose input
0001 = General-purpose input - inverted polarity
0010 = General-purpose output driving low
0011 = General-purpose output driving high
0100 = Status output – non-inverted polarity
0101 = Status output - inverted polarity of the status bit it follows
0110 = Status output – 0 drives low, 1 high impedance
0111 = Status output – 0 high impedance, 1 drives low
1000 to 1111 = {unused values}

Note that the bits of the following registers cannot be internally connected to a GPIO configured as a status output: GPIOSR.

Register Name: GPIOCR2
Register Description: GPIO Configuration Register 2
Register Address: 0Ch

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	GPIO3C[3:0]				GPIO2C[3:0]			
Default	0	0	0	0	0	0	0	0

These fields are identical to those in GPIOCR1 except they control GPIO2 and GPIO3.

Register Name: GPIO0SS
Register Description: GPIO0 Status Select Register
Register Address: 0Dh

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	REG[4:0]					BIT[2:0]		
Default	0	0	0	0	0	0	0	0

Bits 7 to 3: Status Register (REG[4:0]). When GPIOCR1.GPIO0C=01xx, this field specifies the register of the status bit that GPIO0 will follow while the BIT field below specifies the status bit within the register. Setting the combination of this field and the BIT field below to point to a bit that isn't implemented as a real-time or latched status register bit results in GPIO0 being driven low. The address of the status bit that GPIO0 follows is 0x40 + REG[4:0]

Bits 2 to 0: Status Bit (BIT[2:0]). When GPIOCR1.GPIO0C=01xx, the REG field above specifies the register of the status bit that GPIO0 will follow while this field specifies the status bit within the register. Setting the combination of the REG field and this field to point to a bit that isn't implemented as a real-time or latched status register bit results in GPIO1 being driven low. 000=bit 0 of the register. 111=bit 7 of the register.

Note: The device does not allow the GPIO status register bits in GPIOSR to be followed by a GPIO.

Register Name: GPIO1SS
Register Description: GPIO1 Status Select Register
Register Address: 0Eh

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	REG[4:0]					BIT[2:0]		
Default	0	0	0	0	0	0	0	0

These fields are identical to those in GPIO0SS except they control GPIO1.

Register Name: GPIO2SS
Register Description: GPIO2 Status Select Register
Register Address: 0Fh

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	REG[4:0]					BIT[2:0]		
Default	0	0	0	0	0	0	0	0

These fields are identical to those in GPIO0SS except they control GPIO2.

Register Name: GPIO3SS
Register Description: GPIO3 Status Select Register
Register Address: 10h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	REG[4:0]					BIT[2:0]		
Default	0	0	0	0	0	0	0	0

These fields are identical to those in GPIO0SS except they control GPIO3.

Register Name: I2CA
Register Description: I2C Address register 1
Register Address: 11h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	0	I2CA[6:0]						
Default	0	1	1	1	0	1	See below	

Bits 6 to 0: I2C Address (I2CA[6:0]). This field specifies the device's address on the I²C bus. At the assertion of the RSTN pin, bits 6:2 are set to the default values shown above, and bits 1:0 are set to the states of the IF1 and IF0 pins. The MCR1.HRST and MCR1.SRST bits have no effect on these bits. After reset these bits can be written by system software to change the device's I²C address as needed. Note: the value I2CA=0 is invalid.

5.3.2 Status Registers

Register Name: ID1
Register Description: Device Identification Register, MSB
Register Address: 30h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	IDU[7:0]							
Default	0	0	0	1	1	1	see below	

Bits 7 to 0: Device ID Upper (IDU[7:0]). This field is the upper eight bits of the device ID.

Register Name: ID2
Register Description: Device Identification Register, LSB and Revision
Register Address: 31h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	IDL[3:0]				REV[3:0]			
Default	see below				contact factory			

Bits 7 to 4: Device ID Lower (IDL[3:0]). This field is the lower four bits of the device ID.
ZL40250 = 0x1C8
ZL40251 = 0x1E8
ZL40252 = 0x1C9
ZL40253 = 0x1E9

Bits 3 to 0: Device Revision (REV[3:0]). These bits are the device hardware revision starting at 0.

Register Name: CFGSR
Register Description: Configuration Status Register
Register Address: 40h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	CFGD	—	IF[1:0]		TEST	AC[2:0]		
Default	0	0	see below		see below	see below		

`

Bit 7: Configured (CFGD). This read-only bit is cleared by assertion of RSTN, MCR1.HRST or MCR1.SRST and set when any register is written (by auto-configuration or through the processor interface). CFGD=1 indicates that the device register set is no longer in factory-default state, and, therefore, the device must be reset before a GUI-generated configuration script is executed.

Bits 5 to 4: Interface Mode (IF[1:0]). These read-only bits are the latched state of the IF1/MISO and IF0/CSN pins when the RSTN pin transitions high. See section 4.2.

Bit 3: Test Mode (TEST). This read-only bit is the latched state of the TEST/GPIO3 pin when the RSTN pin transitions high or the MCR1.HRST bit is deasserted. For proper operation it should be 0. See section 4.2.

Bits 2 to 0: Auto-Configuration (AC[2:0]). These bits are the latched state of the AC2/GPIO2, AC1/GPIO1 and AC0/GPIO0 pins when the RSTN pin transitions high or the MCR1.HRST bit is deasserted. See section 4.2.

Register Name: GPIOSR
Register Description: GPIO Status Register
Register Address: 41h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	GPIO3L	GPIO2L	GPIO1L	GPIO0L	GPIO3	GPIO2	GPIO1	GPIO0
Default	0	0	0	0	pin state	pin state	pin state	pin state

Bit 7: GPIO3 Change Latched Status (GPIO3L). This latched status bit is set to 1 when the GPIO3 status bit changes state, low-to-high or high-to-low. GPIO3L is cleared when written with a 1. When GPIO3L is set it can cause an interrupt request if the GPIO3IE interrupt enable bit is set.

Bit 6: GPIO2 Change Latched Status (GPIO2L). This latched status bit is set to 1 when the GPIO2 status bit changes state, low-to-high or high-to-low. GPIO2L is cleared when written with a 1. When GPIO2L is set it can cause an interrupt request if the GPIO2IE interrupt enable bit is set.

Bit 5: GPIO1 Change Latched Status (GPIO1L). This latched status bit is set to 1 when the GPIO1 status bit changes state, low-to-high or high-to-low. GPIO1L is cleared when written with a 1. When GPIO1L is set it can cause an interrupt request if the GPIO1IE interrupt enable bit is set.

Bit 4: GPIO0 Change Latched Status (GPIO0L). This latched status bit is set to 1 when the GPIO0 status bit changes state, low-to-high or high-to-low. GPIO0L is cleared when written with a 1. When GPIO0L is set it can cause an interrupt request if the GPIO0IE interrupt enable bit is set.

Bit 3: GPIO3 State (GPIO3). This real-time status bit indicates the current state of the GPIO3 pin, not influenced by any inversion that may be specified by GPIOCR2.GPIO3C.

0 = low
1 = high

Bit 2: GPIO2 State (GPIO2). This real-time status bit indicates the current state of the GPIO2 pin, not influenced by inversion that may be specified by GPIOCR2.GPIO2C.

0 = low
1 = high

Bit 1: GPIO1 State (GPIO1). This real-time status bit indicates the current state of the GPIO1 pin, not influenced by inversion that may be specified by GPIOCR1.GPIO1C.

0 = low
1 = high

Bit 0: GPIO0 State (GPIO0). This real-time status bit indicates the current state of the GPIO0 pin, not influenced by inversion that may be specified by GPIOCR1.GPIO0C.

0 = low
1 = high

Register Name: INTSR
Register Description: Interrupt Status Register
Register Address: 42h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	—	OC	—	—	—	INTIE	INT
Default	0	0	0	0	0	0	0	0

Bit 5: Output Clock Interrupt Status (OC). This read-only bit is set if any of the output clock interrupt status bits are set in the OCISR1 register. See section 4.8.

Bit 1: Interrupt Enable Bit (INTIE). This is the global interrupt enable bit. When this bit is 0 all interrupt sources are prevented from setting the INT global interrupt status bit (below). See section 4.8.

0 = Interrupts are disabled at the global level
1 = Interrupts are enabled at the global level

Bit 0: Interrupt Status (INT). This read-only bit is set when the OC bit in this INTSR register is set and the INTIE bit is set. It is also set by GPIO latched status bits that have their corresponding interrupt enable bits set. This bit can cause an interrupt request when set by configuring one of the GPIO pins to follow it. See section 4.8.

0 = No interrupt
1 = An unmasked interrupt source is active

Register Name: GLOBISR
Register Description: Global Functions Interrupt Status Register
Register Address: 43h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	BCDONE	—	—	—	GPIO3IE	GPIO2IE	GPIO1IE	GPIO0IE
Default	see below	0	0	0	0	0	0	0

Bit 7: Boot Controller Done (BCDONE). This bit indicates the status of the on-chip boot controller, which performs auto-configuration from ROM or EEPROM. It is cleared when the device is reset and set after the boot controller finishes auto-configuration of the device. See section 4.11.

Note that BCDONE cannot be polled while the device is auto-configuring because the internal register bus is in use. The BCDONE bit was designed to be followed by a GPIO pin configured as a status output. To cause GPIO0, for example, to follow BCDONE, include the following settings at the beginning of the auto-configuration script: GPIOCR1=0x04 (configures GPIO0 as a non-inverted status output) and GPIO0SS=00011 111b (causes GPIO0 to follow the bit at register 0x43, bit 7, which is BCDONE).

Alternately, there is a way to poll the device to determine whether auto-configuration is complete. This involves choosing a writeable bit that (a) has a harmless effect, such as GLOBISR.GPIO3IE, and (b) is not set during auto-configuration. System software can then poll the device by writing the register to set the bit then reading the register to see if the bit is set. The bit cannot be set by system software while the device is auto-configuring. Therefore when it is found to be set auto-configuration must be complete.

Bit 3: GPIO3 Change Interrupt Enable (GPIO3IE). This bit enables the GPIOSR.GPIO3L latched status bit to send an interrupt request into the device's interrupt logic.
0 = Interrupt is disabled
1 = Interrupt is enabled

Bit 2: GPIO2 Change Interrupt Enable (GPIO2IE). This bit enables the GPIOSR.GPIO2L latched status bit to send an interrupt request into the device's interrupt logic.
0 = Interrupt is disabled
1 = Interrupt is enabled

Bit 1: GPIO1 Change Interrupt Enable (GPIO1IE). This bit enables the GPIOSR.GPIO1L latched status bit to send an interrupt request into the device's interrupt logic.
0 = Interrupt is disabled
1 = Interrupt is enabled

Bit 0: GPIO0 Change Interrupt Enable (GPIO0IE). This bit enables the GPIOSR.GPIO0L latched status bit to send an interrupt request into the device's interrupt logic.
0 = Interrupt is disabled
1 = Interrupt is enabled

Register Name: OCISR1
Register Description: Output Clock Interrupt Status Register 1
Register Address: 45h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	OC8	OC7	OC6	OC5	OC4	OC3	OC2	OC1
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: Output Clock x Interrupt Status (OC[8:1]). Each bit indicates the current status of the interrupt sources for the corresponding output. It is set when any latched status bit in the OCxSR register is set and the associated interrupt enable bit is also set. See section 4.8.

Register Name: OCISR2
Register Description: Output Clock Interrupt Status Register 2
Register Address: 46h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	—	—	—	—	—	OC10	OC9
Default	0	0	0	0	0	0	0	0

See the OCISR1 register description above.

Register Name: P1SR
Register Description: Path 1 Status Register
Register Address: 48h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	—	—	—	—	—	—	SELREF
Default	0	0	0	0	0	0	0	0

Bit 0: Selected Reference (SELREF). This real-time status field indicates Path 1's selected reference. See section 4.5.

0 = The input specified by P1CR3.MUX
1 = The input specified by P1CR3.ALTMUX

Register Name: P2SR
Register Description: Path 2 Status Register
Register Address: 49h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	—	—	—	—	—	—	SELREF
Default	0	0	0	0	0	0	0	0

Bit 0: Selected Reference (SELREF). This real-time status field indicates Path 2's selected reference. See section 4.5.

0 = The input specified by P2CR3.MUX
1 = The input specified by P2CR3.ALTMUX

Register Name: OCxSR
Register Description: Output Clock x Status Register
Register Address: OC1: 50h, OC2: 51h, OC3: 52h, OC4: 53h, OC5: 54h
OC6: 55h, OC7: 56h, OC8: 57h, OC9: 58h, OC10: 59h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	LSCLKIE	LSCLKL	LSCLK	STARTIE	STARTL	STOPIE	STOPL	STOPD
Default	0	0	0	0	0	0	0	0

Bit 7: (LSCLKIE). This bit enables the LSCLKL latched status bit to send an interrupt request into device's interrupt logic.
0 = Interrupt is disabled
1 = Interrupt is enabled

Bit 6: (LSCLKL). This latched status bit is set when the low-speed divider output clock transitions low-to-high. Writing a 1 to this bit clears it.
0 = Low speed output clock has not transitioned low to high
1 = Low speed output clock has transitioned low to high

Bit 5: (LSCLK). This real-time status bit follows the level of the low-speed divider output clock when the OCxCR3.SRLSEN bit is set.
0 = LSCLK is high
1 = LSCLK is low

Bit 4: (STARTIE). This bit enables the STARTL latched status bit to send an interrupt request into device's interrupt logic.
0 = Interrupt is disabled
1 = Interrupt is enabled

Bit 3: (STARTL). This latched status bit is set when the output clock signal has been started after being stopped. Writing a 1 to this bit clears it. See section 4.6.6.
0 = Output clock signal has not resumed from being stopped
1 = Output clock signal has resumed from being stopped

Bit 2: (STOPIE). This bit enables the STOPL latched status bit to send an interrupt request into device's interrupt logic.
0 = Interrupt is disabled
1 = Interrupt is enabled

Bit 1: (STOPL). This latched status bit is set when the output clock signal has been stopped. Writing a 1 to this bit clears it. See section 4.6.6.
0 = Output clock signal has not stopped
1 = Output clock signal has stopped

Bit 0: (STOPD). This real-time status bit is high when the output clock signal is stopped and low when the output clock is not stopped. See section 4.6.6.
0 = Output clock signal is not stopped
1 = Output clock signal is stopped

5.3.3 Path 1 Configuration Registers

Register Name: P1CR1
Register Description: Path Configuration Register 1
Register Address: 100h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	DALIGN	EXTSS[1:0]		—	—	1	—
Default	0	0	0	0	0	0	1	0

Bit 6: Align Output Dividers (DALIGN). A 0-to-1 transition on this bit causes a simultaneous reset of the medium-speed dividers and the low-speed dividers for all output clocks where OCxCR1.PHEN=1. After this reset all PHEN=1 output clocks with frequencies that are exactly integer multiples of one another will be rising-edge aligned as specified by their OCxPH registers. This bit should be set then cleared once during system startup. Setting this bit during normal system operation can cause phase jumps in the output clock signals.

Bits 5 to 4: External Switch Source Select (EXTSS[1:0]). This field selects the GPIO source for the external switch control signal. It is only valid when P1CR3.EXTSW=1. See section 4.5.

00 = GPIO0
01 = GPIO1
10 = GPIO2
11 = GPIO3

Register Name: P1CR3
Register Description: Path 1 Configuration Register 3
Register Address: 102h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	EXTSW	ALTMUX[2:0]			MUX[2:0]		
Default	0	0	0	0	0	0	1	1

Bit 6: Path 1 External Switching Mode (EXTSW). This bit enables Path 1 external reference switching mode. In this mode, if the selected GPIO signal is low the Path 1 input mux is controlled by P1CR3.MUX. If the selected GPIO signal is high the Path 2 input mux is controlled by P1CR3.ALTMUX. P1CR1.EXTSS specifies which GPIO pin controls this behavior. See section 4.5.

Bits 5 to 3: Path 1 Alternate Mux Control (ALTMUX[2:0]). This field specifies the alternate Path 1 clock source for external switching (when EXTSW=1). See section 4.5.

000 = IC1 input (default)
001 = IC2 input
010 = IC3 input
011 = XA input
100-111 = {reserved values}

Bits 2 to 0: Path 1 Mux Control (MUX[2:0]). By default this field controls the Path 1 input mux. It also specifies the primary Path 1 clock source for external switching (when EXTSW=1). See section 4.5.

000 = IC1 input
001 = IC2 input
010 = IC3 input
011 = XA input (default)
100-111 = {reserved values}

5.3.4 Path 2 Configuration Registers

Register Name: P2CR1
Register Description: Path 2 Configuration Register 1
Register Address: 180h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	DALIGN	EXTSS[1:0]		—	—	1	—
Default	0	0	0	0	0	0	1	0

Bit 6: Align Output Dividers (DALIGN). A 0-to-1 transition on this bit causes a simultaneous reset of the medium-speed dividers and the low-speed dividers for all output clocks where OCxCR1.PHEN=1. After this reset all PHEN=1 output clocks with frequencies that are exactly integer multiples of one another will be rising-edge aligned as specified by their OCxPH registers. This bit should be set then cleared once during system startup. Setting this bit during normal system operation can cause phase jumps in the output clock signals.

Bits 5 to 4: External Switch Source Select (EXTSS[1:0]). This field selects the GPIO source for the external switch control signal. It is only valid when P2CR3.EXTSW=1. See section 4.5.

00 = GPIO0
01 = GPIO1
10 = GPIO2
11 = GPIO3

Register Name: P2CR3
Register Description: Path 2 Configuration Register 3
Register Address: 182h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	EXTSW	ALTMUX[2:0]			MUX[2:0]		
Default	0	0	0	0	0	0	1	1

Bit 6: Path 2 External Switching Mode (EXTSW). This bit enables Path 2 external reference switching mode. In this mode, if the selected GPIO signal is low the Path 2 input mux is controlled by P2CR1.MUX. If the selected GPIO signal is high the Path 2 input mux is controlled by P2CR1.ALTMUX. P2CR1.EXTSS specifies which GPIO pin controls this behavior. See section 4.5.

Bits 5 to 3: Path 2 Alternate Mux Control (ALTMUX[2:0]). This field specifies the alternate Path 2 clock source for external switching (when EXTSW=1). See section 4.5.

000 = IC1 input (default)
001 = IC2 input
010 = IC3 input
011 = XA input
100-111 = {reserved values}

Bits 2 to 0: Path 2 Mux Control (MUX[2:0]). By default this field controls the Path 2 input mux. It also specifies the primary Path 2 clock source for external switching (when EXTSW=1). See section 4.5.

000 = IC1 input
001 = IC2 input
010 = IC3 input
011 = XA input (default)
100-111 = {reserved values}

5.3.5 Output Clock Configuration Registers

Register Name: OCxCR1
Register Description: Output Clock x Configuration Register 1
Register Address: OC1: 200h, OC2: 210h, OC3: 220h, OC4: 230h, OC5: 240h
OC6: 250h, OC7: 260h, OC8: 270h, OC9: 280h, OC10: 290h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	PHEN	MSDIV[6:0]						
Default	0	0	0	0	0	0	0	0

Bit 7: Phase Alignment Enable (PHEN). This bit enables this output to participate in phase alignment. See section 4.6.5.

0 = Phase alignment disabled for this output
1 = Phase alignment enabled for this output

Bits 6 to 0: Medium-Speed Divider Value (MSDIV[6:0]). This field specifies the setting for the output clock's medium-speed divider. The divisor is MSDIV+1. Note that if MSDIV is not set to 0 (bypass) then the maximum input clock frequency to the medium-speed divider is 750MHz and the maximum output clock frequency from the medium-speed divider is 375MHz. When MSDIV=0, the medium-speed divider, phase adjust, low-speed divider, start/stop and output duty cycle adjustment circuits are bypassed and the high-frequency clock signal is sent to the directly output driver. See section 4.6.2.

Register Name: OCxCR2
Register Description: Output Clock x Configuration Register 2
Register Address: OC1: 201h, OC2: 211h, OC3: 221h, OC4: 231h, OC5: 241h
OC6: 251h, OC7: 261h, OC8: 271h, OC9: 281h, OC10: 291h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	POL	DRIVE[1:0]		OCSF[3:0]			
Default	0	0	0	0	0	0	0	0

Bit 6: Clock Path Polarity (POL). The clock path to the output driver is inverted when this bit set. This does not invert the LSDIV path to the CMOS OCxN pin if that path is enabled. See section 4.6.1.

Bits 5 to 4: CMOS/HSTL Output Drive Strength (DRIVE[1:0]). The CMOS/HSTL output drivers have four equal sections that can be enabled or disabled to achieve four different drive strengths from 1x to 4x. When the output power supply VDDOx is 3.3V or 2.5V, the user should start with 1x and only increase drive strength if the output is highly loaded and signal transition time is unacceptable. When VDDOx is 1.8V or 1.5V the user should start with 4x and only decrease drive strength if the output signal has unacceptable overshoot. See section 4.6.1.

00 = 1x
01 = 2x
10 = 3x
11 = 4x

Bits 3 to 0: Output Clock Signal Format (OCSF[3:0]). See section 4.6.1.

0000 = Disabled (high-impedance, low power mode)
0001 = LVDS (V_{OD} is forced to 400mV and OCxDIFF.VOD is ignored)
0010 = Differential (default is LVPECL with V_{CM}=1.2V, programmable using OCxDIFF fields)
0011 = HSTL (set OCxCR2.DRIVE=11 (4x) to meet JESD8-6)
0100 = Two CMOS: OCxN in phase with OCxP
0101 = One CMOS: OCxP enabled, OCxN high impedance
0110 = One CMOS: OCxP high impedance, OCxN enabled
0111 = Two CMOS: OCxN inverted vs. OCxP
1010 = HCSL

Register Name: OCxDIFF
Register Description: Output Clock x Start Stop Register
Register Address: OC1: 202h, OC2: 212h, OC3: 222h, OC4: 232h, OC5: 242h
OC6: 252h, OC7: 262h, OC8: 272h, OC9: 282h, OC10: 292h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	VCM[3:0]				VOD[3:0]			
Default	0	0	0	0	0	1	0	1

Bits 7 to 4: Differential Common-Mode Voltage (VCM[3:0]). This field specifies the common-mode voltage for the differential output driver. See section 4.6.1.

0000 = 1.23V (default) – typical for LVDS and AC-coupled LVPECL
0011 = 1.0V
0100 = 1.1V
0101 = 1.3V
0110 = 1.4V
0111 = 1.5V
1000 = 1.6V
1001 = 1.7V
1010 = 1.8V
1011 = 1.9V
1100 = 2.0V – typical for DC-coupled LVPECL
1101 = 2.1V
1111 = Use this setting for HCSL signal format
All other values reserved

Bits 3 to 0: Differential Swing Voltage (VOD[3:0]). This field specifies the differential output voltage (V_{OD}) for the differential output driver. In the device this field actually controls driver output current. When the specified current is driven into the required external 100Ω termination resistor, the voltage across the termination resistor is the desired V_{OD}. See Figure 15 for the definition of V_{OD}. V_{OD} is equivalent to the single-ended voltage swing of the OCxP pin or the OCxN pin. This field is ignored and V_{OD} is set to 400mV when OCxCR2.OCSF=0001 (LVDS). See section 4.6.1.

0000 = 300mV (3mA driver current)
0001 = 400mV – typical for LVDS
0010 = 500mV
0011 = 600mV
0100 = 700mV
0101 = 800mV – default value, typical for LVPECL
0110 = 900mV (9mA driver current)
1010 = Use this setting for HCSL signal format
All other values reserved

Register Name: OCxREG
Register Description: Output Clock x Regulator Control Register
Register Address: OC1: 203h, OC2: 213h, OC3: 223h, OC4: 233h, OC5: 243h
OC6: 253h, OC7: 263h, OC8: 273h, OC9: 283h, OC10: 293h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	—	—	—	VREG[3:0]			
Default	0	0	0	0	0	0	0	0

Bits 3 to 0: Regulator Voltage (VREG[3:0]). This field specifies the power supply regulator voltage for the differential output driver. Set this to at least VCM+VOD/2+0.5V. Max value is 2.2V when VDDOx is 2.5V, and max value is 2.9V when VDDOx is 3.3V. See section 4.6.1.

0000 = 2.2V (default) – typical for LVDS and AC-coupled LVPECL
0010 = 2.0V
0011 = 2.2V
0100 = 2.25V
0101 = 2.4V
0111 = 2.5V
1000 = 2.7V
1001 = 2.75V
1010 = 2.8V
1011 = 2.9V – typical for DC-coupled LVPECL
1100 = 3.0V
1111 = Use this setting for HCSL signal format
All other values reserved

Register Name: OCxCR3
Register Description: Output Clock x Configuration Register 3
Register Address: OC1: 204h, OC2: 214h, OC3: 224h, OC4: 234h, OC5: 244h
OC6: 254h, OC7: 264h, OC8: 274h, OC9: 284h, OC10: 294h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	SRLSEN	—	NEGLSD	LSSEL	—	—	—	LSDIV[24]
Default	0	0	0	0	0	0	0	0

Bit 7: Enable LSDIV Statuses (SRLSEN). This bit enables the OCxSR.LSCLK real-time status bit and its associated latched status bit OCxSR.LSCLKL.

0 = LSCLK status bit is not enabled (low)
1 = LSCLK status bit is enabled

Bit 5: OCxN Low Speed Divider (NEGLSD). This bit selects the source of the clock on the OCxN pin in CMOS mode. See section 4.6.2.

0 = Same as OCxP
1 = Output of the LSDIV divider

Note: NEGLSD should only be set to one in two-CMOS mode (OCxCR2.OCSF=100 or 111), when OCxCR2.POL=0, and when OCxCR3.LSSEL=0.

Bit 4: LSDIV Select (LSSEL). This bit selects the source of the output clock. When the MSDIV divider is selected (LSSEL=0) the LSDIV divider output can be independently selected as the source for the OCxN pin (in CMOS output mode) or monitored by the OCxSR.LSCLK status bit. This bit is only valid when OCxCR1.MSDIV > 0. See section 4.6.2.

0 = The output clock is sourced from the MSDIV divider.
1 = The output clock is sourced from the LSDIV divider.

Bit 0: Low-Speed Divider Value (LSDIV[24]). See the OCxDIV1 register description.

Register Name: OCxDIV1
Register Description: Output Clock x Divider Register 1
Register Address: OC1: 205h, OC2: 215h, OC3: 225h, OC4: 235h, OC5: 245h
OC6: 255h, OC7: 265h, OC8: 275h, OC9: 285h, OC10: 295h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	LSDIV[7:0]							
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: Low-Speed Divider Value (LSDIV[7:0]). The full 25-bit LSDIV[24:0] field spans this register, OCxDIV2, OCxDIV3. and bit 0 of OCxCR3. LSDIV is an unsigned integer. The frequency of the clock from the medium-speed divider is divided by LSDIV+1. The OCxCR3.LSSEL and NEGLSD bits control when the output of the low-speed divider is present on the OCxP and OCxN output pins. OCxCR1.MSDIV must be > 0 for the low-speed divider to operate. See section 4.6.2.

Register Name: OCxDIV2
Register Description: Output Clock x Divider Register 2
Register Address: OC1: 206h, OC2: 216h, OC3: 226h, OC4: 236h, OC5: 246h
OC6: 256h, OC7: 266h, OC8: 276h, OC9: 286h, OC10: 296h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	LSDIV[15:8]							
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: Low-Speed Divider Value (LSDIV[15:8]). See the OCxDIV1 register description.

Register Name: OCxDIV3
Register Description: Output Clock x Divider Register 3
Register Address: OC1: 207h, OC2: 217h, OC3: 227h, OC4: 237h, OC5: 247h
OC6: 257h, OC7: 267h, OC8: 277h, OC9: 287h, OC10: 297h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	LSDIV[23:16]							
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: Low-Speed Divider Value (LSDIV[23:16]). See the OCxDIV1 register description.

Register Name: OCxDC
Register Description: Output Clock x Duty Cycle Register
Register Address: OC1: 208h, OC2: 218h, OC3: 228h, OC4: 238h, OC5: 248h
OC6: 258h, OC7: 268h, OC8: 278h, OC9: 288h, OC10: 298h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	OCDC[7:0]							
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: Output Clock Duty Cycle (OCDC[7:0]). This field controls the output clock signal duty cycle when MSDIV>0 and LSDIV>1. When OCDC = 0 the output clock is 50%. Otherwise the clock signal is a pulse with a width of OCDC number of MSDIV output clock periods. The range of OCDC can create pulse widths from 1 to 255 MSDIV output clock periods. When OCxCR2.POL=0, the pulse is high and the signal is low the remainder of the cycle. When POL=1, the pulse is low and the signal is high the remainder of the cycle. See section 4.6.3.

Register Name: OCxPH
Register Description: Output Clock x Phase Adjust Register
Register Address: OC1: 209h, OC2: 219h, OC3: 229h, OC4: 239h, OC5: 249h
OC6: 259h, OC7: 269h, OC8: 279h, OC9: 289h, OC10: 299h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	—	—	—	PHADJ[3:0]			
Default	0	0	0	0	0	0	0	0

Bits 3 to 0: Phase Adjust Value (PHADJ[3:0]). This field can be used to adjust the phase of an output clock vs. the phase of other clock outputs. The adjustment is in units of bank source clock cycles. For example, if the bank source clock is 625MHz then one bank source clock cycle is 1.6ns, the smallest phase adjustment is 0.8ns, and the adjustment range is ±5.6ns. Negative values mean earlier in time (leading) and positive values mean later in time (lagging). See section 4.6.4.

0000 = 0 bank source clock cycles
0001 = 0.5
0010 = 1.0
0011 = 1.5
0100 = 2.0
0101 = 2.5
0110 = 3.0
0111 = 3.5
1000 = -1.0 bank source clock cycles
1001 = -0.5
1010 = -2.0
1011 = -1.5
1100 = -3.0
1101 = -2.5
1110 = -4.0
1111 = -3.5

Register Name: OCxSTOP
Register Description: Output Clock x Start Stop Register
Register Address: OC1: 20Ah, OC2: 21Ah, OC3: 22Ah, OC4: 23Ah, OC5: 24Ah
OC6: 25Ah, OC7: 26Ah, OC8: 27Ah, OC9: 28Ah, OC10: 29Ah

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	SRC[3:0]				NEGLSD	MODE[1:0]	
Default	0	0	0	0	1	1	0	0

Bits 6 to 3: Output Clock Stop Source (SRC[3:0]). This field specifies the source of the stop signal. See section 4.6.6.

0000 = Never stop
0001 = Logical OR of (the global MCR1.STOP bit) or (the OCx stop bit in the STOPCR registers)
0010 to 0111 = {unused values}
1000 = GPIO0
1001 = GPIO1
1010 = GPIO2
1011 = GPIO3
1100 to 1111 = {unused values}

Bit 2: NEGLSD Stop Behavior (NEGLSD). When an output pair is configured for two different frequencies in 2xCMOS mode (see section 4.6.2) this bit specifies the stop behavior for the pair. This field allows the user to trade off stop reaction time vs. possible short pulse on the NEG pin.

0 = Stop when higher-speed POS signal has the appropriate edge (see MODE field below)
1 = Stop when lower-speed NEG signal has the appropriate edge.

Setting this bit to 1 guarantees no short high/low time for the POS signal and for the NEG signal, but stopping can take a long time when the NEG pin is very low frequency, such as 2kHz or even 1Hz.

Setting this bit to 0 allows stopping to happen faster because it depends only on the frequency of the POS signal, but the NEG signal may have a short high or low time when it stops. For some applications, such as when NEG is

a 1 pulse per second (PPS) signal, a short high or low time when NEG stops may not matter because NEG is essentially a data signal (phase alignment or time alignment signal that is latched by a POS signal edge) rather than a true clock signal.

Bits 1 to 0: Output Clock Stop Mode (MODE[1:0]). This field selects the mode of the start-stop function. See section 4.6.6.

00 = Stop Low: stop after falling edge of output clock, start after rising edge of output clock
01 = Stop High: stop after rising edge of output clock, start after falling edge of output clock
10 = Stop Low then go high-impedance: stop after falling edge, start after rising edge
11 = Stop High then go high-impedance: stop after rising edge, start after falling edge

The following table shows which pin(s) stop high or low as specified above for each output signal format:

Signal Format	OCxCR2.OCSF	Pin that Stops As Specified
LVDS, LVPECL, Programmable Differential	001 or 010	OCxP
HSTL	011	OCxP
Two CMOS, OCxP in phase with OCxN	100	OCxP and OCxN
One CMOS, OCxN enabled	101	OCxN
One CMOS, OCxP enabled	110	OCxP
Two CMOS, OCxN inverted vs. OCxP	111	OCxP

5.3.6 Input Clock Configuration Registers

Register Name: XACR1
Register Description: XA Input Clock Configuration Register 1
Register Address: 300h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	POL	—	—	—	—	HSDIV[1:0]	
Default	0	0	0	0	0	0	0	0

Bit 6: Input Polarity (POL). This field specifies whether the device as an inversion in the input signal path.

0 = Normal
1 = Inverted

Bits 1 to 0: Input Clock High-Speed Divider (HSDIV[1:0]). This field specifies the divide value for the XA input clock divider. See Figure 1.

00 = Divide by 1
01 = Divide by 2
10, 11 = {unused values}

Register Name: XACR2
Register Description: XA Input Clock Configuration Register 2
Register Address: 301h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	XOAMP[7:0]							
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: XO Amplifier Control (XOAMP[7:0]). Set this value as follows for the recommended 10pF crystal (values in decimal). Contact Microsemi apps support for XOAMP values for crystals with other load capacitances.

Crystal Frequency (MHz)	Max Crystal Drive		
	100µW	200µW	300µW
25	0	80	152
30	0	72	136
35	0	72	136
40	8	80	136
45	8	80	136
50	16	88	136
55	16	88	136
60	24	96	136

Register Name: XACR3
Register Description: XA Input Clock Configuration Register 3
Register Address: 302h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	XBCAP[3:0]				XACAP[3:0]			
Default	0	0	0	0	0	0	0	0

Bits 7 to 4: XB Internal Capacitor Selection (XBCAP[3:0]). Actual internal capacitance on the XB pin in pF is approximately 6 + XBCAP. See section 4.3.2.

Bits 3 to 0: XA Internal Capacitor Selection (XACAP[3:0]). Actual internal capacitance on the XA pin in pF is approximately 6 + XACAP. See section 4.3.2.

Register Name: ICxCR1
Register Description: Input Clock x Configuration Register 1
Register Address: IC1: 303h, IC2: 304h, IC3: 305h

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Name	—	POL	—	—	—	—	HSDIV[1:0]	
Default	0	0	0	0	0	0	0	0

Bit 6: Input Polarity (POL). This field specifies whether the device as an inversion in the input signal path.
0 = Normal
1 = Inverted

Bits 1 to 0: Input Clock High-Speed Divider (HSDIV[1:0]). This field specifies the divide value for the input clock high-speed divider. See Figure 1.
00 = Divide by 1
01 = Divide by 2
10 = Divide by 4
11 = Divide by 8

6. Electrical Characteristics

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Supply voltage, nominal 1.5V	VDD15	-0.3	1.65	V
Supply voltage, nominal 1.8V	VDD18	-0.3	1.98	V
Supply voltage, nominal 2.5V	VDD25	-0.3	2.75	V
Supply voltage, nominal 3.3V	VDD33	-0.3	3.63	V
Voltage on XA, any ICxP/N, any OCxP/N pin	VANAPIN	-0.3	3.63	V
Voltage on any digital I/O pin	VDIGPIN	-0.3	3.63	V
Storage Temperature Range	T_{ST}	-55	+125	°C

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.
* Voltages are with respect to ground (VSS) unless otherwise stated.

Note 1: The typical values listed in the tables of Section 6 are not production tested.
Note 2: Specifications to -40°C and 85°C are guaranteed by design or characterization and not production tested.

Table 5 - Recommended DC Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units
Supply voltage, Higher Core (choose 1 row)	VDDH	2.375	2.5	2.625	V
		3.135	3.3	3.465	
Supply voltage, Lower Core (choose 1 row)	VDDL	1.71	1.8	1.89	V
		same as VDDH			
Supply voltage, Non-Clock I/O Pins (choose 1 row)	VDDIO	1.71 2.375	1.8 2.5	1.89 2.625	V
		same as VDDH			
Supply voltage, OCx Outputs (x=A,B,C,D,E or F) (choose 1 row)	VDDOx	1.425 1.71 2.375	1.5 1.8 2.5	1.575 1.89 2.625	V
		same as VDDH			
Operating temperature	T_A	-40		+85	°C

Table 6 - Electrical Characteristics: Supply Currents

Characteristics	Symbol	Min.	Typ.[1]	Max	Units	Notes
Total power, one input and one LVDS output enabled, XA/XB disabled, 1.8V+3.3V operation	P_{DISS}		0.187		W	
3.3V single-supply operation Total current on 3.3V supply	I_{DD33}		334	516	mA	Note 2
2.5V single-supply operation Total current on 2.5V supply	I_{DD25}		325	510	mA	Note 2
1.8V+3.3V operation Total current on 3.3V supply Total current on 1.8V supply	 I_{DD33} I_{DD18}		 66 186	 170 284	mA	Note 2
1.8V+2.5V operation Total current on 2.5V supply Total current on 1.8V supply	 I_{DD25} I_{DD18}		 64 186	 162 292	mA	Note 2
VDDH supply current change from enabling or disabling the crystal driver circuit	ΔI_{DDXO}		13		mA	
VDDL supply current change from enabling or disabling an input clock	ΔI_{DDLIN}		12		mA	
VDDL supply current from enabling/disabling output divider for one OCx using OCEN.OCxEN	ΔI_{DDLDIV}		13		mA	
VDDL supply current change from enabling or disabling an output for LVDS, LVPECL or HCSL	ΔI_{DDLD}		13		mA	

Characteristics	Symbol	Min.	Typ.[1]	Max	Units	Notes
VDDL supply current change from enabling or disabling an output for CMOS or HSTL	ΔI_{DDLC}		16		mA	
VDDOx supply current change from enabling or disabling an LVDS output	ΔI_{DDOD}		9		mA	
VDDOx supply current change from enabling or disabling an LVPECL output	ΔI_{DDOP}		15		mA	
VDDOx supply current change from enabling or disabling an HCSL output	ΔI_{DDOHC}		15		mA	Note 5
VDDOx supply current change from enabling or disabling a CMOS output	ΔI_{DDOC}		6		mA	Note 3
VDDOx supply current change from enabling or disabling an HSTL output	ΔI_{DDOHS}		6		mA	Note 4

Note 1: Typical values measured at nominal supply voltages and 25°C ambient temperature.

Note 2: Max I_{DD} measurements made with all blocks enabled, 625MHz signals on IC1 and IC2 inputs, 156.25MHz signal on IC3, Crystal driver off , all MSDIV dividing by 2, all LSDIV dividing by 2, and outputs enabled as LVPECL outputs driving 156.25MHz signals, and all VDDO at same voltage as VDDH. Typical I_{DD} measurements made with same setup as max I_{DD} but only six outputs enabled with LVDS signal format.

Note 3: VDDOx=3.3V, 1x drive strength, f_O=250MHz, 2pF load

Note 4: VDDOx=1.8V, 2x drive strength, f_O=100MHz, 100Ω differential termination.

Note 5: 50Ω to ground each on OCxP and OCxN.

Table 7 - Electrical Characteristics: Non-Clock CMOS Pins

Characteristics		Symbol	Min.	Typ.	Max.	Units	Notes
Input high voltage		V_{IH}	0.7 x VDDIO			V	
Input low voltage		V_{IL}			0.3 x VDDIO	V	
Input leakage current, all digital inputs		I_{IL}	-10		10	µA	Note 1
Input capacitance		C_{IN}		3	10	pF	
Input capacitance, SCL/SCLK, SDA/MOSI		C_{IN}		3	11	pF	
Input hysteresis, SCL and SDA in I^2C Bus Mode			0.05 x VDDIO			mV	
Output leakage (when high impedance)		I_{LO}	-10		10	µA	Note 1
Output high voltage		V_{OH}	0.8 x VDDIO			V	I_O = -3.0mA
Output low voltage		V_{OL}			0.2 x VDDIO	V	I_O = 3.0mA
Clock output on GPIO pin, frequency		f_{OUT}			50	MHz	Note 3
Clock output on GPIO pin, rise/fall time	VDDIO=1.8V	t_R, t_F		2.3		ns	Notes 3, 4
	VDDIO=2.5V			1.5		ns	Notes 3, 4
	VDDIO=3.3V			1.2		ns	Notes 3, 4

Note 1: 0V < V_{IN} < VDDIO for all other non-clock inputs.

Note 2: V_{OH} does not apply for SCL and SDA in I^2C interface mode since they are open drain.

Note 3: To output a clock on a GPIO pin, an OCx output must be configured with NEGLSD=1 and SRLSEN=1 in OCxCR3 and the GPIO must be configured to as a status output following OCxSR.LSCLK (see the GPIOCR and GPIOxSS registers). Output jitter is not guaranteed for clock signals on GPIO pins but is typically 1 to 5ps rms 12kHz to 20MHz.

Note 4: 20%-80%, 15pF load.

Table 8 - Electrical Characteristics: XA Clock Input

This table covers the case when there is no external crystal connected and an external oscillator or clock signal is connected to the XA pin.

Characteristics	Symbol	Min.	Typ.	Max.	Units	Notes
Input high voltage, XA	V_{IH}	1.2		VDDH	V	VDDH=2.5 or 3.3V
Input low voltage, XA	V_{IL}			0.8	V	VDDH=2.5 or 3.3V
Input frequency, XA pin	f_{IN}			156.25	MHz	
Input leakage current	I_{IL}	-10		10	µA	
Input duty cycle		40		60	%	1.0V threshold

Table 9 - Electrical Characteristics: Clock Inputs, ICxP/N

Characteristics	Symbol	Min.	Typ.	Max.	Units	Notes
Input voltage tolerance (each pin, single-ended)	V_{TOL}	0		VDDH	V	Note 1
Input differential voltage	V_{ID}	0.1		1.4	V	Note 2
Input DC bias voltage (internally biased)	V_{CMI}		1.35		V	
Input frequency, ICx pins	f_{IN}			1250	MHz	Differential
				300	MHz	Single-ended
Minimum input clock high, low time, $f_{IN} \leq 250MHz$	t_H, t_L		smaller of 3ns or 0.3 x 1 / f_{IN}		ns	
Minimum input clock high, low time, $250MHz \leq f_{IN} \leq 750MHz$	t_H, t_L		0.4*1 / f_{IN}		ns	
Minimum input clock high, low time, $f_{IN} \geq 750MHz$	t_H, t_L		0.45*1 / f_{IN}		ns	
Input resistance, single-ended to 1.8V, ICxP or ICxN	R_{IN18}		50		kΩ	
Input resistance, single-ended to VSS, ICxP or ICxN	R_{INVSS}		80		kΩ	

Note 1: The device can tolerate voltages as specified in V_{TOL} w.r.t. VSS on its ICxP and ICxN pins without being damaged. For differential input signals, proper operation of the input circuitry is only guaranteed when the other specifications in this table, including V_{ID}, are met.

Note 2: For inputs IC1P/N and IC2P/N $V_{ID}=|V_{ICxP} - V_{ICxN}|$. For input IC3P, $V_{ID}=|V_{IC3P} - V_{CMI}|$. The max V_{ID} spec only applies when a differential signal is applied on ICxP/N; it does not apply when a single-ended signal is applied on ICxP.

Note 3: **Differential signals.** The differential inputs can easily be interfaced to neighboring ICs driving LVDS, LVPECL, CML, HCSL, HSTL or other differential signal formats using a few external passive components. In general, Microsemi recommends terminating the signal with the termination/load recommended in the neighboring component's data sheet and then AC-coupling the signal into the ICxP/ICxN pins. See Figure 14 for details. To connect a differential signal to IC3, AC-couple one side of the signal to IC3P and AC-couple the other side to VSS. For DC-coupling, treat the input as 1.8V CML.

Note 4: **Single-ended signals** can be connected to the ICxP pins. Signals with amplitude greater than 2.5V must be DC-coupled. For signals with amplitudes less than 2.5V Microsemi recommends AC-coupling but DC-coupling can also be used. When a single-ended signal is connected to ICxP, ICxN should be connected to a capacitor (0.1µF or 0.01µF) to VSS.

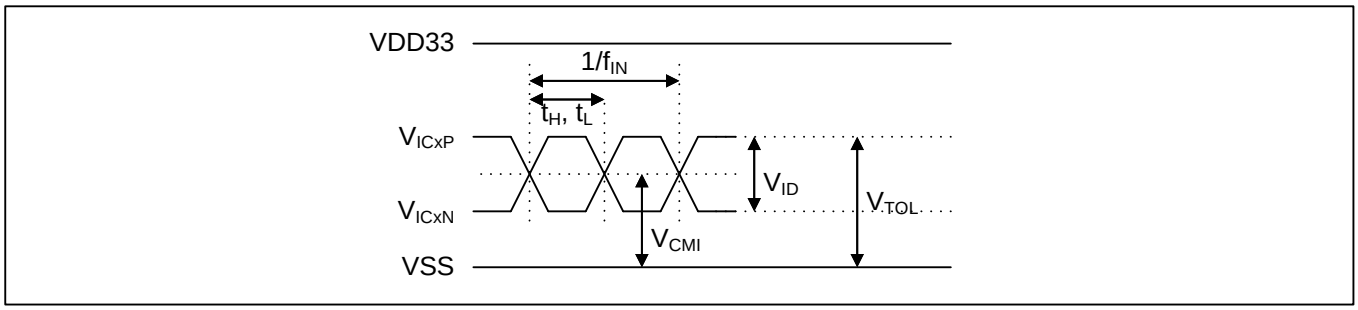


Figure 13 - Electrical Characteristics: Clock Inputs

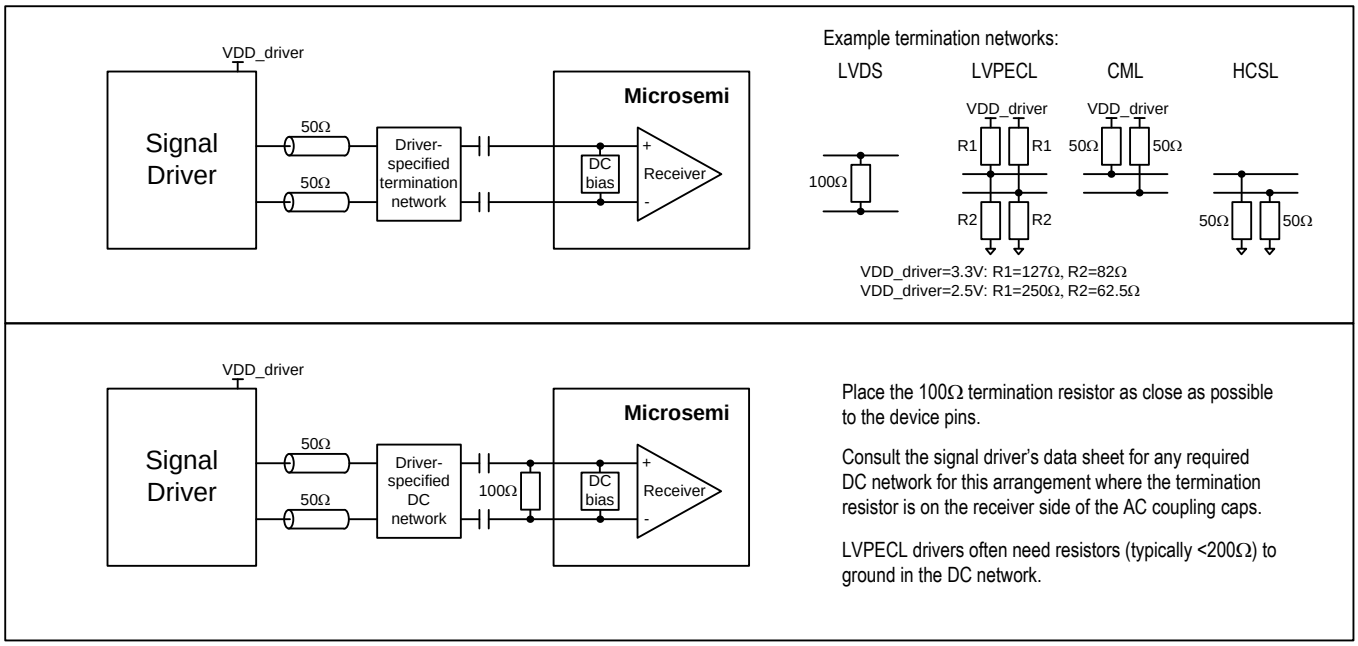


Figure 14 - Example External Components for Differential Input Signals

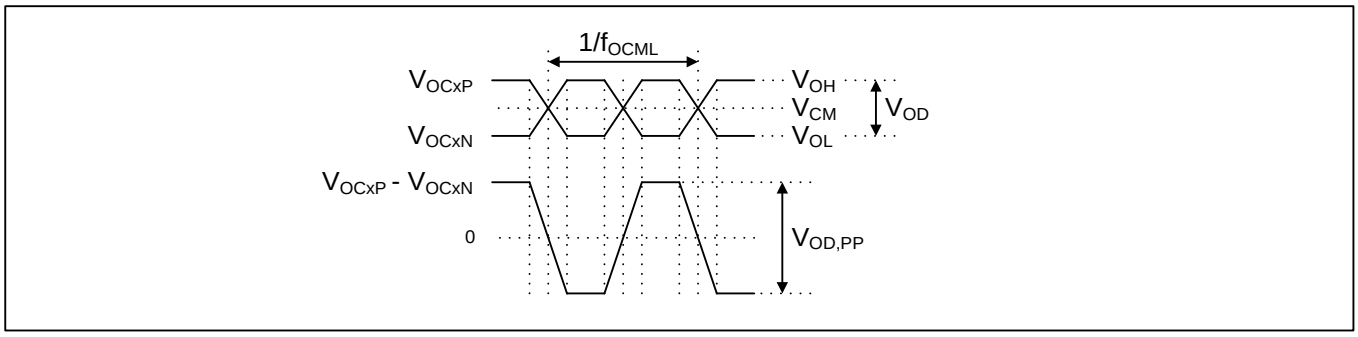


Figure 15 - Electrical Characteristics: Differential Clock Outputs

Table 10 - Electrical Characteristics: LVDS Clock Outputs

VDDOx = 2.5V±5% or 3.3V±5% for LVDS operation.

Characteristics	Symbol	Min.	Typ.	Max.	Units	Notes
Output frequency	f_{OCD}			1045	MHz	
Output common-mode voltage	V_{CM}	1.13	1.2	1.37	V	Note 1. See Figure 15
Output differential voltage	V_{OD}	310	420	530	mV	Note 1. See Figure 15
Output differential swing, peak-to-peak	$V_{OD,PP}$	620	840	1060	mV_{PP}	Note 1. See Figure 15
Output rise/fall time	t_R, t_F		150		ps	20%-80%
Output duty cycle		45	50	55	%	

Note 1: OCxCR2.OCSF=0001 (LVDS). Output must have 100Ω DC path between OUTxP and OUTxN to meet these V_{OD} specs**.** See Figure 16 parts a) and b) for examples where this DC path is a 100Ω termination resistor at the receiver

Table 11 - Electrical Characteristics: LVPECL Clock Outputs

VDDOx = 2.5V±5% or 3.3V±5% for LVPECL operation.

Characteristics	Symbol	Min.	Typ.	Max.	Units	Notes
Output frequency	f_{OCD}			1045	MHz	
Output common-mode voltage, VDDOx=3.3V	V_{CM}	1.85	1.95	2.05	V	Note 1. See Figure 15
Output common-Mode voltage, VDDOx=2.5V	V_{CM}	1.13	1.23	1.33	V	Note 1. See Figure 15
Output differential voltage	V_{OD}	650	820	1050	mV	Note 1. See Figure 15
Output differential swing, peak-to-peak	V_{OD}	1300	1640	2100	mV_{PP}	Note 1. See Figure 15
Output rise/fall time	t_R, t_F		150		ps	20%-80%
Output duty cycle		45	50	55	%	

Note 1: OCxCR2.OCSF=0010, OCxDIFF.VCM=1100, OCxDIFF.VOD=0101. Output must have 100Ω DC path between OUTxP and OUTxN to meet these V_{OD} specs**.** See Figure 16 parts a) and b) for examples where this DC path is a 100Ω termination resistor at the receiver.

Table 12 - Electrical Characteristics: HCSL Clock Outputs

VDDOx=VDDH=3.3V±5% or VDDOx=VDDH=2.5V±5% for HCSL operation.

Characteristics	Symbol	Min.	Typ.	Max.	Units	Notes
Output frequency	f_{OCHC}			250	MHz	
Output common-mode voltage	V_{CM}		V_{OD} / 2		V	Note 1. See Figure 15
Output differential voltage	V_{OD}	0.6	0.75	0.95	V	Note 1. See Figure 15
Output rise/fall time	t_R, t_F		250		ps	20%-80%
Output duty cycle		45	50	55	%	

Note 1: Each of OCxP and OCxN with 50Ω termination resistor to ground.

Table 13 - Electrical Characteristics: CMOS and HSTL (Class I) Clock Outputs

Characteristics	Symbol	Min.	Typ.	Max.	Units	Notes
Output frequency	f_{OCMOS}	<<1Hz		250	MHz	Note 1
Output high voltage	V_{OH}	VDDOx –0.4		VDDOx	V	Notes 2, 3
Output low voltage	V_{OL}	0		0.4	V	Notes 2, 3
Output rise/fall time, VDDOx=1.8V, OCxCR2.DRIVE=4x	t_R, t_F		0.4		ns	2pF load
Output rise/fall time, VDDOx=1.8V, OCxCR2.DRIVE=4x			1.2		ns	15pF load
Output rise/fall time, VDDOx=3.3V, OCxCR2.DRIVE=1x			0.7		ns	2pF load
Output rise/fall time, VDDOx=3.3V, OCxCR2.DRIVE=1x			2.2		ns	15pF load
Output duty cycle		45	50	55	%	Note 4, 6
Output duty cycle		42	50	58	%	Notes 5, 6
Output duty cycle, OCxNEG single-ended			50		%	
Output duty cycle, OCxPOS single-ended			50		%	
Output current when output disabled	I_{OH}		300		µA	OCxCR2.OCSF=0

Note 1: Minimum output frequency is a function of VCO frequency and output divider values and is guaranteed by design.

Note 2: For HSTL Class I, V_{OH} and V_{OL} apply for both unterminated loads and for symmetrically terminated loads, i.e. 50Ω to VDDOx/2.

Note 3: For VDDOx=3.3V and OCxCR2.DRIVE=1x, I_O=4mA. For VDDOx=1.5V and OCxCR2.DRIVE=4x, I_O=8mA.

Note 4: Output clock frequency ≤ 160MHz or VDDOx ≥ 1.8V.

Note 5: Output clock frequency > 160MHz and VDDOx < 1.8V.

Note 6: Measured differentially.

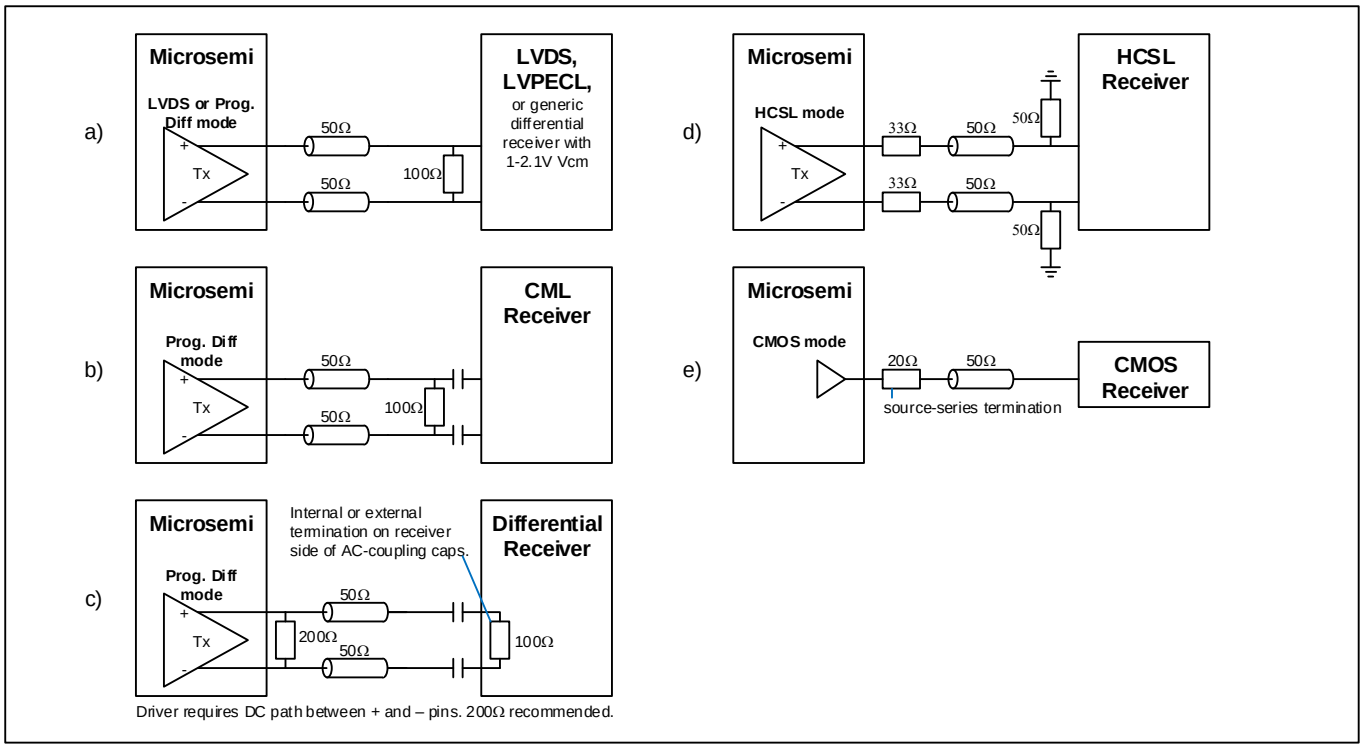


Figure 16 - Example External Components for Output Signals

Figure 16 part c) covers the case where an existing receiver has AC coupling caps followed by an internal or external 100Ω termination resistor. The driver requires a DC path between its POS and NEG pins even in this case. A 200Ω resistor is recommended. Since this arrangement attenuates the signal by one third, The OCxDIFF.VOD field should be set 50% higher to compensate.

Table 14 - Electrical Characteristics: Jitter and Skew Specifications

Characteristics		Min.	Typ.	Max.	Units	Notes
Additive Jitter (Note 7)	100MHz		0.198		ps RMS	Notes 1, 5
	125MHz		0.174			
	156.25MHz		0.155	0.175		
	200MHz		0.141			
	400MHz		0.115			
	800MHz		0.094			
Input-to-Output Propagation Delay, from IC1 or IC2 input		2	2.3	2.6	ns	Note 3
		3	3.4	3.8	ns	Note 4
Input-to-Output Propagation Delay, from IC3 input		1.9	2.3	2.6	ns	Note 3
		2.9	3.4	3.8	ns	Note 4
Input-to-Output Propagation Delay, from XA input		2.9	3.3	3.7	ns	Note 3
		3.9	4.4	4.9	ns	Note 4
Output-to-Output Skew			60	100	ps	Note 2
Output Phase Jitter, 50MHz crystal, 50MHz output			0.29		ps RMS	Notes 5, 6
Output Period Jitter, 50MHz crystal, 50MHz output			11		ps pk-pk	N=10000, Note 6
Output Cycle-to-Cycle Jitter, 50MHz crystal, 50MHz output			11		ps pk	N=10000, Note 6

Note 1: Output frequency = input frequency, LVPECL output signal format.

Note 2: Only applies for outputs that have the same signal format, VDDO voltage, drive strength and load/termination. Also, this skew spec doesn't apply to OCxN when an output pair is configured with OCxCR3NEGLSD=1; in this configuration OCxN lags OCxP by up to 1ns.

Note 3: Differential outputs with 100Ω differential termination (LVDS, LVPECL, Programmable Differential).

Note 4: CMOS/HSTL outputs, 5pF load.

Note 5: Jitter calculated from integrated phase noise from 12kHz to 20MHz.

Note 6: Tested with 50MHz crystal TXC 7M50070021.

Note 7: Additive jitter contributes in a root-of-sum-of-squares manner. For example, a 156.25MHz input signal with 220fs of jitter will experience typical additive jitter of 155fs in the device, and the resulting output jitter will be sqrt(2202+1552)=269fs.

Table 15 - Electrical Characteristics: SPI Slave Interface Timing, Device Registers

VDDIO = 3.3V±5% or 2.5V±5% or 1.8V±5%

Characteristics (Notes 1 to 3)	Symbol	VDDIO 3.3V or 2.5V			VDDIO 1.8V			Units	Notes
		Min.	Typ.	Max.	Min.	Typ.	Max.		
SCLK frequency	f_{BUS}			23			15	MHz	
SCLK cycle time	t_{CYC}	43.5			66			ns	
CSN setup to first SCLK edge	t_{SUC}	10			10			ns	
CSN hold time after last SCLK edge	t_{HDC}	10			10			ns	
CSN high time	t_{CSH}	25			25			ns	
SCLK high time	t_{CLKH}	10			33			ns	
SCLK low time	t_{CLKL}	21.75			33			ns	
MOSI data setup time	t_{SUI}	2			10			ns	
MOSI data hold time	t_{HDI}	2			10			ns	
MISO enable time from SCLK edge	t_{EN}	0			0			ns	
MISO disable time from CSN high	t_{DIS}			80			80	ns	
MISO data valid time	t_{DV}			20.5			32	ns	
MISO data hold time from SCLK edge	t_{HDO}	0			0			ns	
CSN, MOSI input rise time, fall time	t_R, t_F			10			10	ns	

Note 1: All timing is specified with 100pF load on all SPI pins.

Note 2: All parameters in this table are guaranteed by design or characterization.

Note 3: See timing diagram in Figure 17.

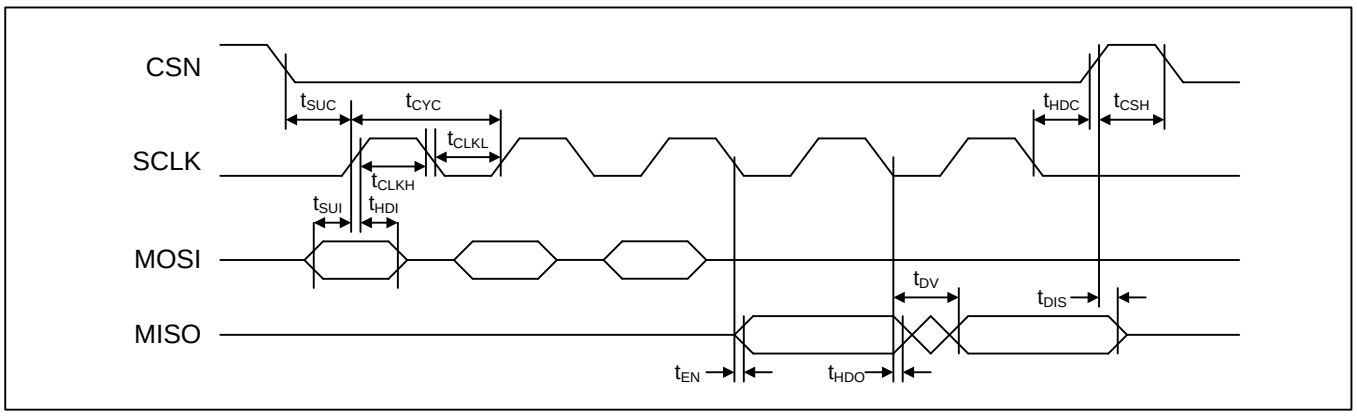


Figure 17 - SPI Slave Interface Timing

Table 16 - Electrical Characteristics: SPI Slave Interface Timing, Internal EEPROM
(ZL40251 and ZL40253 Only)
VDDIO = 3.3V±5% or 2.5V±5% or 1.8V±5%

Characteristics (Notes 1 to 4)	Symb	VDDIO 3.3V		VDDIO 2.5V		VDDIO 1.8V		Units
		Min	Max	Min	Max	Min	Max	
SCLK frequency	f_{BUS}		7.7		4.5		4	MHz
SCLK cycle time	t_{CYC}	130		220		240		ns
CSN setup to first SCLK edge	t_{SUC}	50		100		100		ns
CSN hold time after last SCLK edge	t_{HDC}	53		103		105		ns
CSN high time	t_{CSH}	50		100		100		ns
SCLK high time	t_{CLKH}	40		80		80		ns
SCLK low time	t_{CLKL}	63		107		120		ns
MOSI data setup time	t_{SUI}	11		21		25		ns
MOSI data hold time	t_{HDI}	11		21		25		ns
MISO enable time from SCLK edge	t_{EN}	0		0		0		ns
MISO disable time from CSN high	t_{DIS}		22		22		25	ns
MISO data valid time	t_{DV}		63		107		119	ns
MISO data hold time from SCLK edge	t_{HDO}	0		0		0		ns
CSN, MOSI input rise time, fall time	t_R, t_F		10		10		10	ns

Note 1: This timing applies (a) when EESEL=1 and (b) in direct EEPROM write mode (see section 4.11.2).

Note 2: All timing is specified with 100pF load on all SPI pins.

Note 3: All parameters in this table are guaranteed by design or characterization.

Note 4: See timing diagram in Figure 17.

Table 17 - Electrical Characteristics: SPI Master Interface Timing (ZL40250 and ZL40252 Only)

VDDIO = 3.3V±5% or 2.5V±5% or 1.8V±5%

Characteristics (Notes 1 to 3)	Symbol	Min.	Typ.	Max.	Units	Notes
SCLK output frequency	f_{BUS}			5	MHz	
SCLK output cycle time	t_{CYC}	200			ns	
SCLK output duty cycle	t_{CLKH}/ t_{CYC}	45	50	55	%	
CSN output setup to first SCLK rising edge	t_{SUC}	200			ns	
CSN output hold after last SCLK falling edge	t_{HDC}	200			ns	
CSN output high time	t_{CSH}	200			ns	
MISO input setup time to SCLK rising edge	t_{SU}	15			ns	
MISO input hold time from SCLK rising edge	t_{HD}	5			ns	
MOSI output valid from SCLK falling edge	t_{DV}			10	ns	
SCLK, CSN, MOSI output rise time, fall time	t_R, t_F			15	ns	
MISO input rise time, fall time	t_R, t_F			10	ns	

Note 1: All timing is specified with 100pF load on all SPI pins.

Note 2: All parameters in this table are guaranteed by design or characterization.

Note 3: See timing diagram in Figure 18.

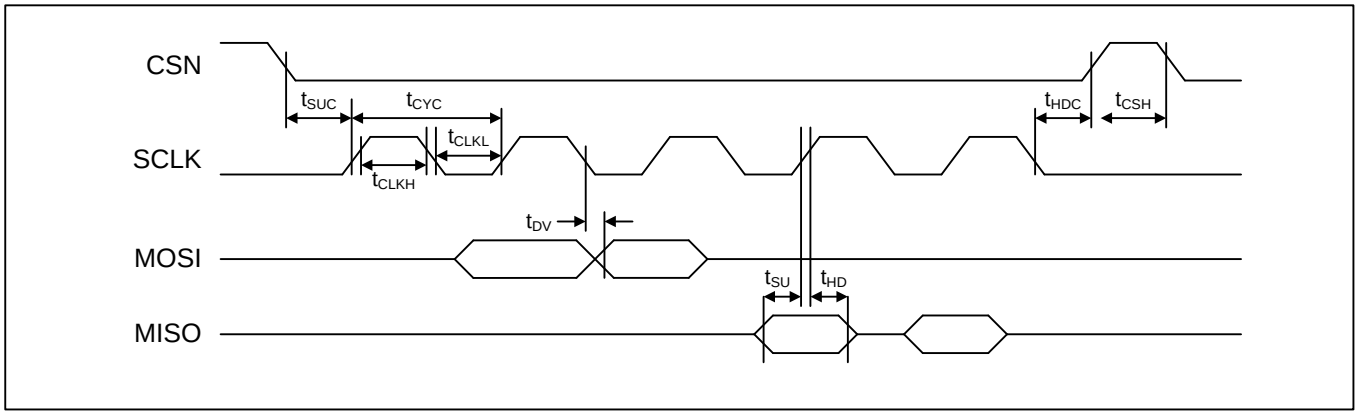


Figure 18 - SPI Master Interface Timing

Table 18 - Electrical Characteristics: I²C Slave Interface Timing

VDDIO = 3.3V±5% or 2.5V±5% or 1.8V±5%

Characteristics	Symbol	Min.	Typ.	Max.	Units	Notes
SCL clock frequency	f_{SCL}			400	kHz	Note 1
Hold time, START condition	$t_{HD:STA}$	0.6			µs	
Low time, SCL	t_{LOW}	1.3			µs	
High time, SCL	t_{HIGH}	0.6			µs	
Setup time, START condition	$t_{SU:STA}$	0.6			µs	
Data hold time	$t_{HD:DAT}$	0		0.9	µs	Notes 2 and 3
Data setup time	$t_{SU:DAT}$	100			ns	
Rise time	t_R				ns	Note 4
Fall time	t_F	$20 + 0.1C_b$		300	ns	C_b is cap. of one bus line
Setup time, STOP condition	$t_{SU:STO}$	0.6			µs	
Bus free time between STOP/START	t_{BUF}	1.3			µs	
Pulse width of spikes which must be suppressed by the input filter	t_{SP}	0		50	ns	

Note 1: The timing parameters in this table are specifically for 400kbps Fast Mode. Fast Mode devices are downward-compatible with 100kbps Standard Mode I²C bus timing. All parameters in this table are guaranteed by design or characterization. All values referred to V_{IHmin} and V_{ILmax} levels (see Table 7).

Note 2: The device internally provides a hold time of at least 300ns for the SDA signal (referred to the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL. Other devices must provide this hold time as well per the I²C specification.

Note 3: The I²C specification indicates that the maximum $t_{HD:DAT}$ spec only has to be met if the device does not stretch the low period (t_{LOW}) of the SCL signal. The device does not stretch the low period of the SCL signal.

Note 4: Determined by choice of pull-up resistor.

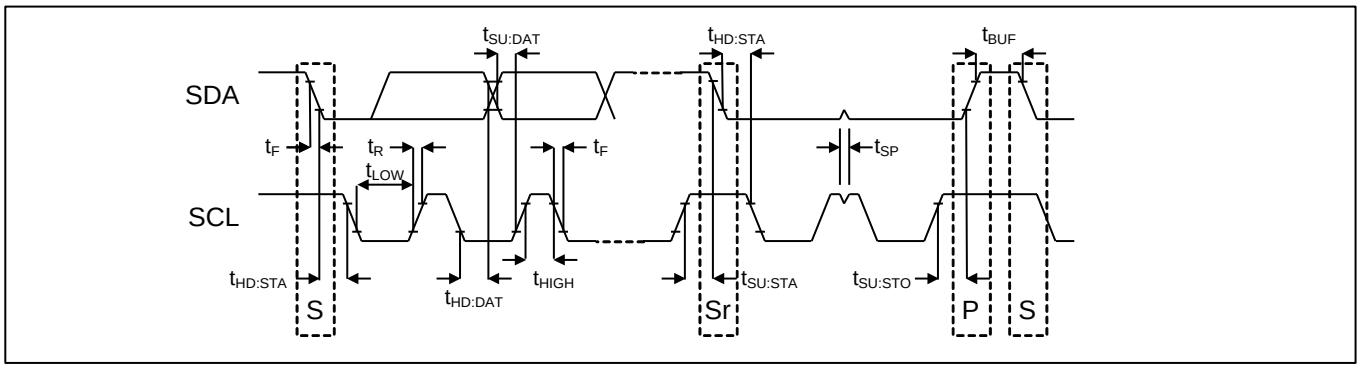


Figure 19 - I²C Slave Interface Timing

7. Package and Thermal Information

Table 19 - 8x8mm QFN Package Thermal Properties

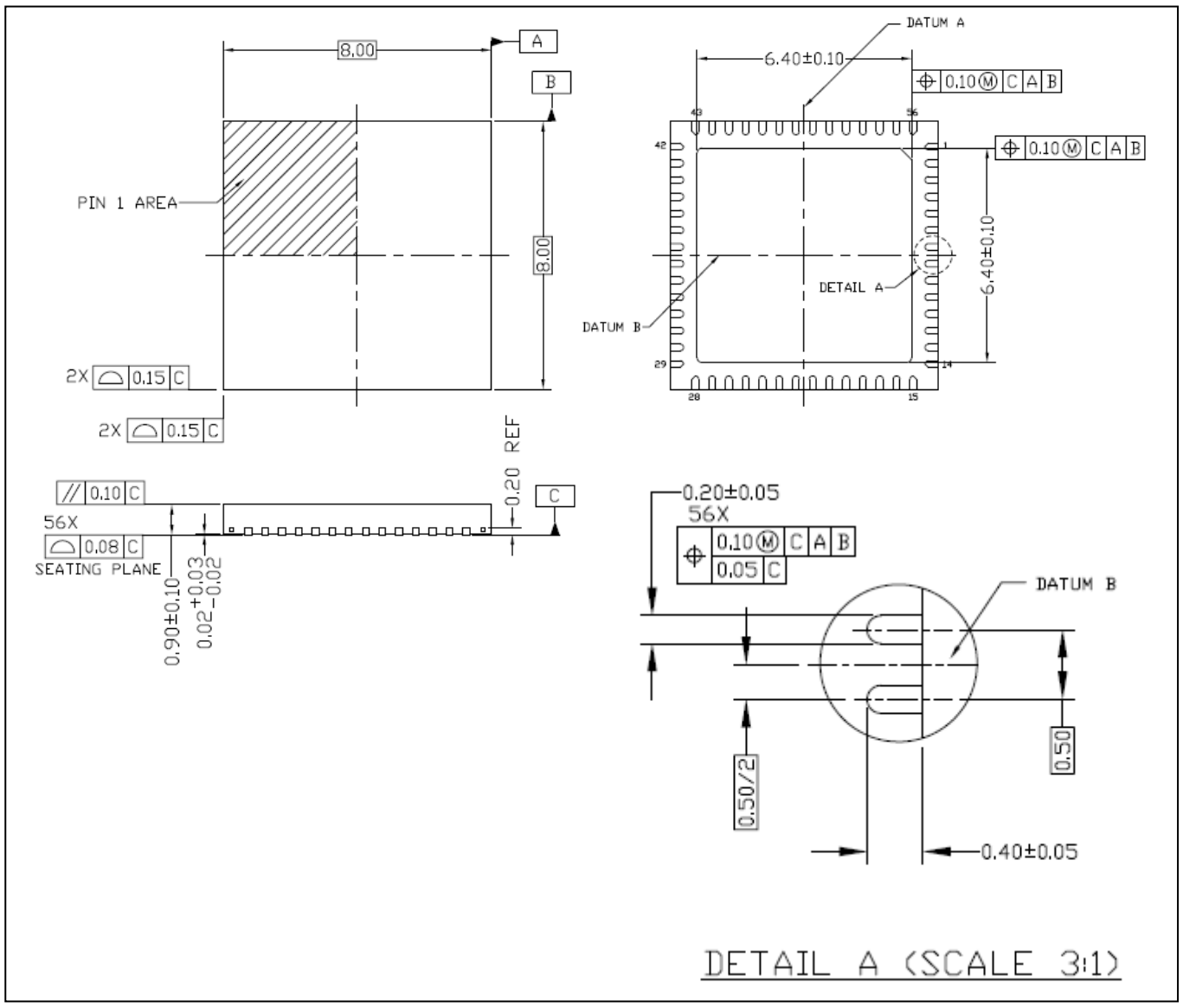
PARAMETER	SYMBOL	CONDITIONS	VALUE	UNITS
Maximum Ambient Temperature	T_A		85	°C
Maximum Junction Temperature	T_{JMAX}		125	°C
Junction to Ambient Thermal Resistance (Note 1)	θ_{JA}	still air	15.1	°C/W
		1m/s airflow	12.4	
		2.5m/s airflow	10.6	
Junction to Board Thermal Resistance	θ_{JB}		3.2	°C/W
Junction to Case Thermal Resistance	θ_{JC}		7.3	°C/W
Junction to Pad Thermal Resistance (Note 2)	θ_{JP}	Still air	0.9	°C/W
Junction to Top-Center Thermal Characterization Parameter	ψ_{JT}	Still air	0.1	°C/W

Note 1: Theta-JA (θ_{JA}) is the thermal resistance from junction to ambient when the package is mounted on an 8-layer JEDEC standard test board and dissipating maximum power.

Note 2: Theta-JP (θ_{JP}) is the thermal resistance from junction to the center exposed pad on the bottom of the package.

Note 3: For all numbers in the table, the exposed pad is connected to the ground plane with a 9x9 array of thermal vias; via diameter 0.33mm; via pitch 0.76mm.

8. Mechanical Drawing



9. Acronyms and Abbreviations

CML	current mode logic
GbE	gigabit Ethernet
HCSL	high-speed current steering logic
HSTL	high-speed transceiver logic
I/O	input/output
LVDS	low-voltage differential signal
LVPECL	low-voltage positive emitter-coupled logic
ppb	parts per billion
ppm	parts per million
pk-pk	peak-to-peak
RMS	root-mean-square
RO	read-only
R/W	read/write
UI	unit interval
UI_{PP} or UI_{P-P}	unit interval, peak to peak
XO	crystal oscillator

10. Data Sheet Revision History

Revision	Description
26-Sep-2016	First general release
08-Dec-2016	In Table 1, OCx pin description, clarified what is programmable for each mode. Added new Figure 16. In Table 14 added min, typ and max values for buffer Input-to-Output Propagation Delay. In footnotes 3 and 4 added “Measured at 125MHz”.
12-Jun-2017	Corrected references to MCR1.XAB to MCR2.XAB. Corrected four occurrences of VCCOx to VDDOx. Added pullup recommendations to SCL/SCLK and SDA/MOSI pin descriptions. Change ID2.REV default value to “contact factory”. In OCxCR2.OCSF HCSL decode, deleted “VCM and VOD are ignored”.
12-Jul-2017	In Table 9 deleted minimum frequency values for f_{IN}.
17-Jul-2017	In Figure 16 removed the 50ohm to ground termination option from the CMOS diagram.
05-Sep-2017	In Table 1 TEST/GPIO3 pin description, changed “TEST must be low on the rising edge of RSTN” to “Typically TEST should be low on the rising edge of RSTN, but see section 4.2 for some options.” In section 4.6.2 added the statement that maximum input frequency to the medium-speed divider is 750MHz. In section 4.9 added new subsection 4.9.1 to guide users in the use of external RC reset circuits.
29-May-2018	On page 1 changed wording to indicate PCIe 1-4 compliance. In OCxCR3.NEGLSD description added to note that OCxCR3.LSSEL must be 0 to set NEGLSD=1.
14-Sept-2018	In Table 14, corrected typo for "Input-to-Output Propagation Delay, from IC3 input" in the Note 4 row where the max of 2.8 was less than typical of 3.4. Corrected the max to 3.8.

Revision	Description
	In the OCxCR2.OCSF description, deleted "(must have VDDOx=VDDH=3.3V)" from the HCSL decode. Updated Table 10 Note 1 and Table 11 Note 1 and added cross reference to Figure 16 parts a) and b). Updated Figure 16 to include new part c) and added noted about part c) below the figure. In section 4.9.1 second paragraph added need for current-limiting series resistor between source of reset signal and device RSTN pin. In Table 1 pin descriptions for AC0/GPIO0, AC1/GPIO1, AC2/GPIO2 and TEST/GPIO3 added note.
29-Sep-2020	In Table 12 changed max V_{OD} from 0.86V to 0.95V, changed min V_{OD} from 0.62V to 0.6V and changed V_{CM} spec to V_{OD} / 2.

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