PRODUCT/PROCESS CHANGE NOTIFICATION

PCN IPG-IPC/14/8648
Dated 08 Aug 2014

PDIP8 ASSEMBLING AND TESTING TRANSFER FROM ST- LONGGANG TO NANTONG FUJTSU SUBCON AND ST-MUAR

Table 1. Change Implementation Schedule

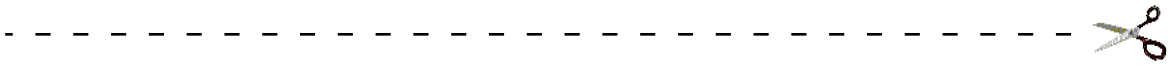
Forecasted implementation date for change	01-Nov-2014
Forecasted availability date of samples for customer	06-Sep-2014
Forecasted date for **STMicroelectronics** change Qualification Plan results availability	01-Sep-2014
Estimated date of changed product first shipment	07-Nov-2014

Table 2. Change Identification

Product Identification (Product Family/Commercial Product)	PDIP 8 products and E-TEA3718SDP in PDIP 16
Type of change	Package assembly location change, Testing location change
Reason for change	Our internal LGG facility is proceeding in a shut down road map.
Description of the change	ST is pursuing the plan to rationalize the manufacturing processes. Because of this, ST is announcing the transfer ot assembling and testing activities originally installed in our Longgang (LGG) facility in China to Nantong Fujtsu (NFME) subcon facility in China. All testing activities originally performed in LGG will be transferred to ST Muar-Malaysia facility. The transfer will impact on all packages families actually present in LGG. More specifically the different PDIP package families will be transferred to the NFME subcon facility. Implementation will occur all along the year, till end of 2014. Packages will be transferred in sequence and depending on Test Vehicles, implemented and released at different time frames within the year.
Change Product Identification	By a new Finished Goods code
Manufacturing Location(s)	

Table 3. List of Attachments

Customer Part numbers list	
Qualification Plan results	



Customer Acknowledgement of Receipt	**PCN IPG-IPC/14/8648**
Please sign and return to STMicroelectronics Sales Office	**Dated 08 Aug 2014**

☐ Qualification Plan Denied	Name:
☐ Qualification Plan Approved	Title:
	Company:
☐ Change Denied	Date:
☐ Change Approved	Signature:

Remark

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DOCUMENT APPROVAL

Name	Function
Chelli, Fabio	Marketing Manager
Conti, Mauro	Marketing Manager
Merisio, Massimiliano	Marketing Manager
Romano, Eugenio	Marketing Manager
Sandrini, Francesca Marta	Marketing Manager
Vavassori, Emanuele	Marketing Manager
Arrigo, Domenico Massimo	Product Manager
Borghi, Maria Rosa	Product Manager
Pioppo, Sergio Franco	Product Manager
Moretti, Paolo	Q.A. Manager

PDIP8 ASSEMBLING AND TESTING TRANSFER FROM ST- LONGGANG TO NANTONG FUJTSU SUBCON AND ST-MUAR

WHAT is the change?

ST is pursuing the plan to rationalize the manufacturing processes. Because of this, ST is announcing the transfer of assembling and testing activities originally installed in our Longgang (LGG) facility in China to Nantong Fujtsu (NFME) subcon facility in China. Majority of the testing activities originally performed in LGG will be transferred to ST Muar-Malaysia facility.
The transfer will impact on all packages families actually present in LGG. More specifically the different PDIP package families will be transferred to the NFME subcon facility. Implementation will occur all along the year, till end of 2014. Packages will be transferred in sequence and depending on Test Vehicles, implemented and released at different time frame within the year.
The transfer will also imply in several cases material changes in view of rationalization. These changes combination are reported with more details within the PCN.

Present PCN is focused on PDIP8 assembling and testing transfer. PCN for PDIP14/16 has been already issued and implementation is on going. PCNs for DIP7 and SDIP10 will be issued later. Because of the nature of transfer, sample availability, qualification reports and initial shipping will occur not simultaneously but along a period of time. Estimated time frames are reported within the PCN.

Package	Impacted Product families	Change of Bill of Material (BOM) compared with previous BOM	Final testing Site/Testing Platform Change
PDIP8 Assy and testing transfer to NFME and ST-Muar	Power Conversion - VIPER12-VIPER22	No material change compared to LGG	Muar Testing site/No testing platform change
	Power Conversion – All other product families	New Molding Compound and New Glue. Reported in the Reliability Report	Muar Testing Site/ No testing platform change
	Industrial and ASICs – All impacted product families	New Molding Compound and New Glue. Reported in the Reliability Report	Muar Testing site/ No testing platform change
	Hand Held and Portable Power Management – All impacted product families	New Molding Compound and New Glue. Reported in the Reliability Report	Muar Testing site/ No testing platform change

WHY:

Our internal LGG facility is proceeding in a shutdown road map. Therefore the related activities will be transferred to other facilities: NFME in Nantong –China (for assembling) and ST- Muar-Malaysia (for final testing).

WHEN will this change occur?

Package	Test vehicles by Commercial Products/Line codes	Test Vehicles Samples availability	Qualification Report availability (upon request)	Estimated First Shipment start date
PDIP 8	VIPER12-VIPER22/VNA4-VNB7	WK31	Final Report WK36	From WK42
	VIPER53-VIPER57/VNH1-VNH6	WK35	Final Report WK48	From WK48
	L6562/UE27	WK31	Final Report WK36	From WK42
	L4971/U738	WK35	Final Report WK46	From WK48
	L6561/U093	WK31	Final Report WK48	From WK48
	L6387E/U324	WK31	Final Report WK48	From WK48
	AVS1ACP08/S131	WK35	Final Report WK48	From WK48
	TDE1798DP/1798	WK35	Final Report WK48	From WK48
	UC3845BN/L127	WK35	Final Report WK46	From WK48
	MC34063/LL02	WK35	Final Report WK48	From WK48
	WFP135P08/WF35	WK35	Final Report WK48	From WK48

HOW will the change be qualified?

- This change will be qualified using the standard STMicroelectronics procedures for quality and reliability. Major steps of the qualification are:
  - Process capability assessment and Workability on all TVs
  - Reliability Trials on all TVs
  - DOE and Corner Lots

- Depending on TVs all or subset of the above qualifications steps criteria will be applied

Test Vehicles	Workability	DOE Corner Lots	Final test Data and Correlation	Reliability Trial
VIPER12-VIPER22/VNA4-VNB7	X	X	X	X
VIPER53-VIPER57/VNH1-VNH6	X	X	X	X
L6562/UE27	X	X	X	X
L4971/U738	X	X	X	X
L6561/U093	X	On similar die	X	X
L6387E/U324	X	X	X	X
AVS1ACP08/S131	X	On similar die	X	X
TDE1798DP/1798	X	On similar die	X	X
UC3845BN/L127	X	X	X	X
MC34063/LL02	X	X	X	X
WFP135P08/WF35	X	X	X	X

IMPACTS OF THE CHANGE:

Form: No change
Fit: No change
Function: No change

APPENDICES:

- APPENDIX 1 Reliability plan for involved Test Vehicles
- APPENDIX 2 Assy transfer to NFME and Testing transfer to Muar: List of Impacted commercial products

ATTACHMENTS:

- **Preliminary Reliability Report on VIPER12-VIPER22**
- **Preliminary Reliability Report on L6562**

APPENDIX 1: RELIABILITY PLAN

Test Vehicles by CP/Line codes	HTOL/HTRB	TEMPERATURE HUMIDITY BIAS	THERMAL CYCLES	PRESSURE POT	HIGH TEMPERATURE STORAGE
VIPER12-VIPER22/VNA4-VNB7	X	X	X	X	X
VIPER53-VIPER57/VNH1-VNH6	X		X	X	X
L6562/UE27	X		X	X	X
L4971/U738			X	X	X
L6561/U093		X	X	X	X
L6387E/U324	X	X	X	X	X
AVS1ACP08/S131			X	X	X
TDE1798DP/1798			X	X	X
UC3845BN/L127			X	X	X
MC34063/LL02			X	X	X
WFP135P08/WF35			X	X	X

Reliability Report

General Information	
Product Line	*VNA4, VNB7*
Product Description	*SMPS PRIMARY I.C, VIPER*
Finished Good Code	*VIPER12A* *VIPER22A*
Product division	*IND.& POWER CONV.*
Package	*PDIP 8*
Silicon process technology	*VIPOWER – M03*
Raw Line Code :	*4F8W*VNA4X3B* *4F8W*VNB7X3A*

Locations	
Wafer fab location	*AMK6 6*
Assembly plant location	NANTONG FUJITSU − CHINA
Reliability plant location	CATANIA
Preliminary Reliability assessment	*POSITIVE*

DOCUMENT HISTORY

Version	Date	Pages	Author	Comment
1.0	23/07/2014	11	A. Vilardo	-

Issued by **Antonio Vilardo**
IPG Rel Dept.– APG Support

Table of Contents

1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
AEC-Q100	Stress test qualification for integrated circuits
8161393	General specification for product development

2 TEST GLOSSARY

TEST NAME	DESCRIPTION	NOTE
AC:	Autoclave at 2atm	
HTSL:	High Temperature Storage Life	
TC:	Temperature Cycling	
HTRB:	High Temperature Reverse Bias Test	

3 RELIABILITY REPORT OVERVIEW

3.1 Objectives

Aim of this report is to present the results of the reliability evaluation performed on VIPER12A and VIPER22A device due to assembly plant location change from LONGGANG to NANTONG FUJITSU

For the reliability evaluation the following tests were carried out:

AC, TC, HTSL, HTRB

In particular three lots were used, two of VIPER12A and one of VIPER22A.

3.2 Conclusion

Preliminary reliability evaluation has been completed with positive results confirmed at final electrical testing.

4 DEVICE CHARACTERISTICS

4.1 Device description

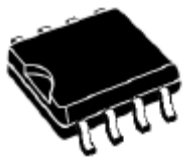
4.1.1 Generalities

Features

- Fixed 60kHZ Switching Frequency
- 9V to 38V Wide Range V_{DD} Voltage
- Current Mode Control
- Auxiliary Undervoltage Lockout with Hysteresis
- High Voltage Start-up Current Source
- Overtemperature, Overcurrent and Overvoltage Protection with Auto-Restart
- Typical power capability
  - European (195 - 265 Vac) 8W for SO-8, 13W for DIP-8
  - European (85 - 265 Vac) 5W for SO-8, 8W for DIP-8

Description

The VIPer12A combines a dedicated current mode PWM controller with a high voltage Power MOSFET on the same silicon chip.



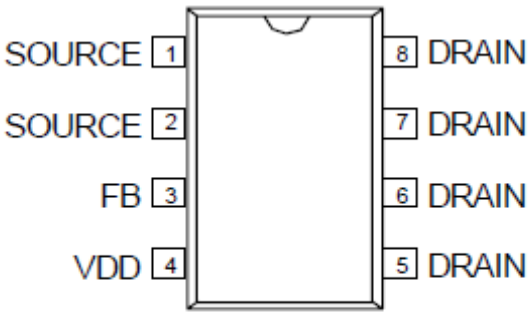
SO-8

DIP-8

Typical applications cover off line power supplies for battery charger adapters, standby power supplies for TV or monitors, auxiliary supplies for motor control, etc.
The internal control circuit offers the following benefits:

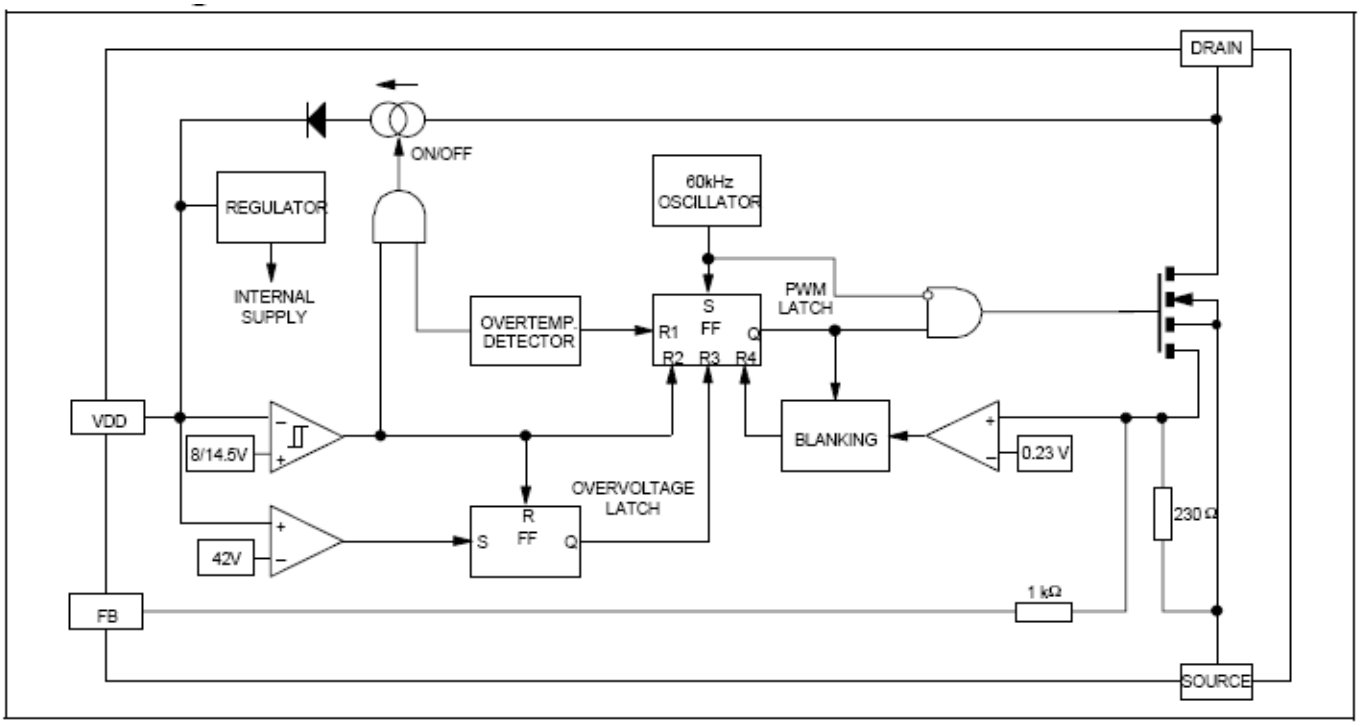
- Large input voltage range on the V_{DD} pin accommodates changes in auxiliary supply voltage. This feature is well adapted to battery charger adapter configurations.
- Automatic burst mode in low load condition.
- Overvoltage protection in HICCUP mode.

4.1.2 Pin connection



DIP-8

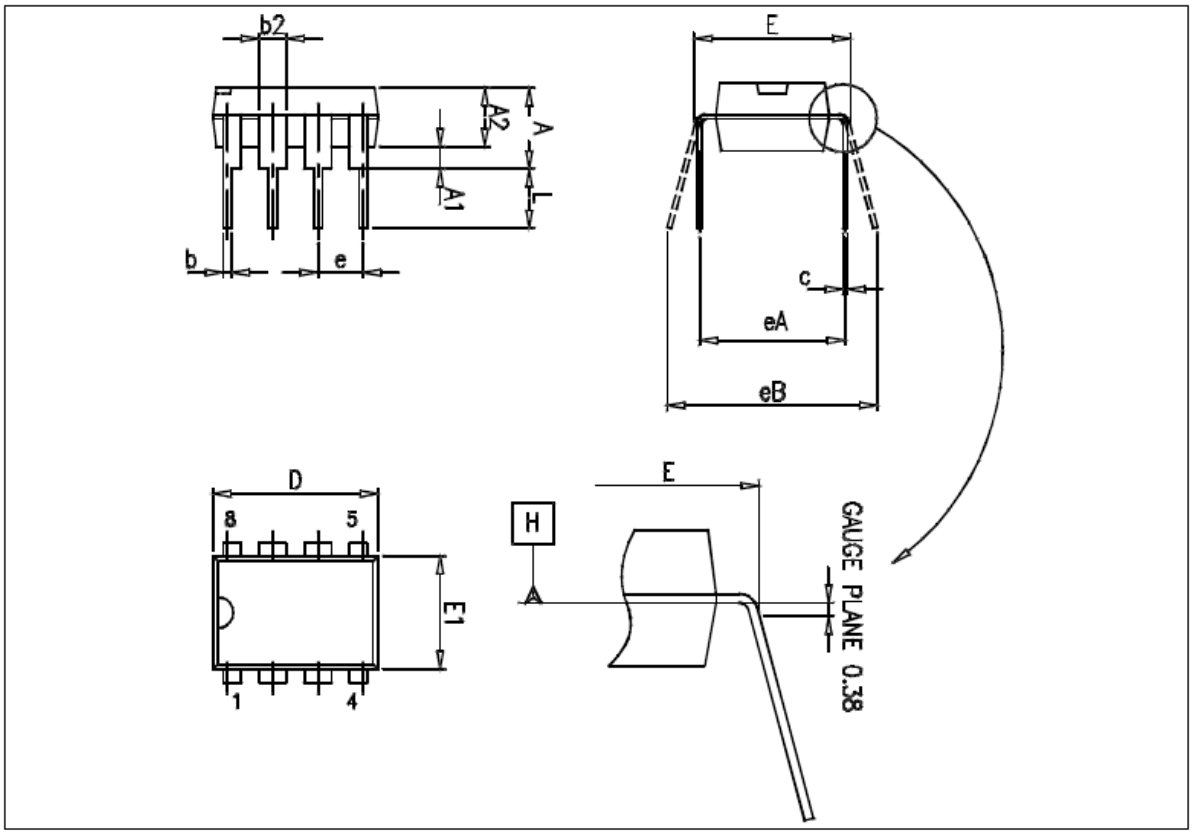
4.1.3 Block diagram



4.1.4 Package outline/Mechanical data

Dimensions			
Ref.	Databook (mm)		
	Nom.	Min	Max
A			5.33
A1	0.38		
A2	2.92	3.30	4.95
b	0.36	0.46	0.56
b2	1.14	1.52	1.78
c	0.20	0.25	0.36
D	9.02	9.27	10.16
E	7.62	7.87	8.26
E1	6.10	6.35	7.11
e		2.54	
eA		7.62	
eB			10.92
L	2.92	3.30	3.81
Package Weight	Gr. 470		

Figure 15. Package Dimensions



4.2. Traceability

Wafer fab information	
Wafer fab manufacturing location	*AMK6 6*
Wafer diameter	*6*
Silicon process technology	*VIPOWER – M03*
Die finishing back side	*Ti/Ni/Au*
Die size (VIPER12A)	*2800 x 2070 micron*
Die size (VIPER22A)	*3250 x 2070 micron*
Passivation	*SiN*
Metal levels	*1*

Assembly Information	
Assembly plant location	*NANTONG FUJITSU − CHINA*
Frame description	*DIP8*
Molding compound	*8390S25*
Wires bonding materials/diameters	*Au (1.3 mils)*
Die attach material	*MG46FAM*

Final Testing Information	
Electrical testing manufacturing location	*LONGGANG -CHINA*

5 TESTS RESULTS SUMMARY

5.1 Test Plan and Results Summary

	Test						
N	**TEST NAME**	**PREC**	**CONDITION/METHOD**	**STEPS**	**1 LOT FAILS/SS**	**2 LOT FAILS/SS**	**3 LOT FAILS/SS**
2	AC	Y	JEDEC MSL = 3 REFLOW PROFILE = Ecopack (Tmax=260°C) LF Ta = 121 Pressure (Atm) = 2 Reference specification = JESD22-A102	0 H	0/77	0/77	0/77
				96 H	0/77	0/77	0/77
3	TC	Y	JEDEC MSL = 3 REFLOW PROFILE = Ecopack (Tmax=260°C) LF Low Ta = -65 High Ta = 150 Reference specification = JESD22-A104	0 CY	0/77	0/77	0/77
				100 CY	0/77	0/77	0/77
				200 CY	-	-	-
				500 CY	-	-	-

	Test						
N	**TEST NAME**	**PREC**	**CONDITION/METHOD**	**STEPS**	**1 LOT FAILS/SS**	**2 LOT FAILS/SS**	**3 LOT FAILS/SS**
4	HTSL	N	Ta = 150 Reference specification = JESD22-A103	0 H	0/77	0/77	0/77
				168 H	0/77	0/77	0/77
				500 H	-	-	-
				1000 H	-	-	-
5	HTRB	Y	Tj = 150°C Reference specification = JESD22-A108	0H	0/54	0/54	0/54
				168 H	0/54	0/54	0/54
				500 H	-	-	-
				1000 H	-	-	-

6 TESTS DESCRIPTION

6.1 Die and Package tests description

TEST NAME	DESCRIPTION	PURPOSE
AC: Autoclave at 2atm	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
HTSL: High Temperature Storage Life	The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.	To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding.
TC: Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, moulding compound delamination, wire-bonds failure, die
HTRB: High Temperature Reverse Bias Test	The device is stressed in static configuration, trying to satisfy as much as possible the following conditions: -) low power dissipation; -) max. supply voltage compatible with diffusion process and internal circuitry limitations;	To maximize the electrical field across either reverse-biased junctions or dielectric layers, in order to investigate the failure modes linked to mobile contamination, oxide ageing, layout sensitivity to surface effects.

Reliability Report

General Information	
Product Line	*UE27*
Product Description	*Transition-mode PFC controller*
Product division	*I&PC*
Package	*PDIP8*
Silicon process technology	*BCD2S*

Locations	
Wafer fab location	*ANG MO KIO*
Assembly plant location	*Nantong Fujitsu - China*
Preliminary Reliability assessment	*Pass*

DOCUMENT HISTORY

Version	Date	Pages	Author	Comment
1.0	17-Jul-14	8	S.O.Cannizzaro	Original document

Issued by

Salvatore Omar Cannizzaro

Approved by

Alceo Paratore

Table of Contents

1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
AEC-Q100	: Stress test qualification for integrated circuits
8161393A	: General Specification For Product Development

2 RELIABILITY EVALUATION OVERVIEW

2.1 Objectives

This report contains the reliability evaluation of UE27 device diffused in ANG MO KIO and assembled in PDIP8 in Nantong Fujitsu - China, included in the overall plan of the transfer from Longgang assy plant to NFME-Fujitsu assy plant.

According to Reliability Qualification Plan, below is the list of the trials performed:

Die Oriented Tests

- High Temperature Operating Life
- High Temperature Reverse Bias

Package Oriented Tests

- Temperature Cycling
- Autoclave
- High Temperature Storage Life

2.2 Conclusion

Taking in account the results of the trials performed on the UE27 device diffused in ANG MO KIO and assembled in PDIP8 in Nantong Fujitsu - China a preliminary positive judgment can be gave out.

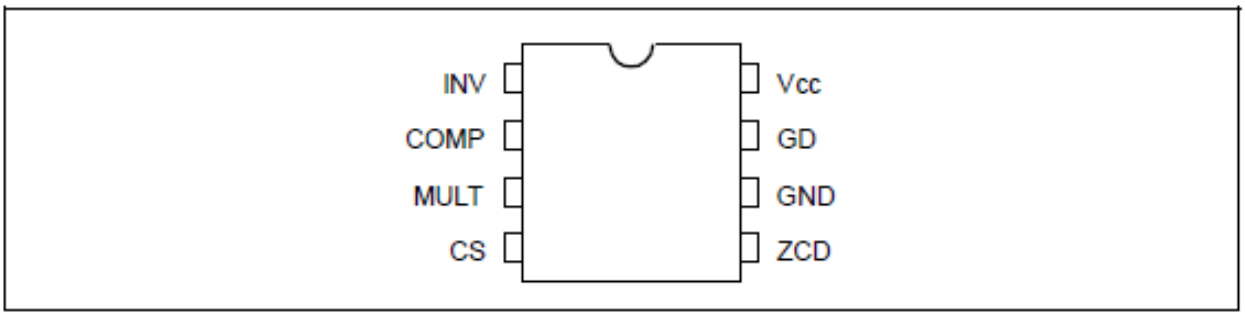
3 DEVICE CHARACTERISTICS

3.1 Device description

3.1.1 Generalities

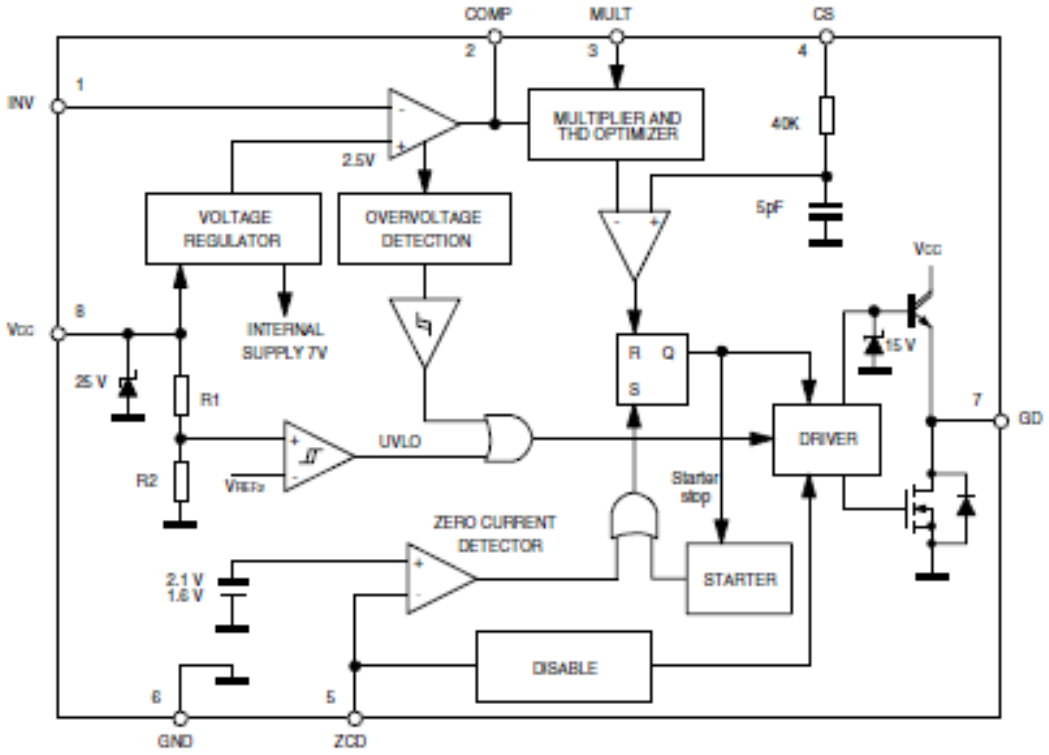
The L6562 is a current-mode PFC controller operating in Transition Mode.

3.1.2 Pin connection

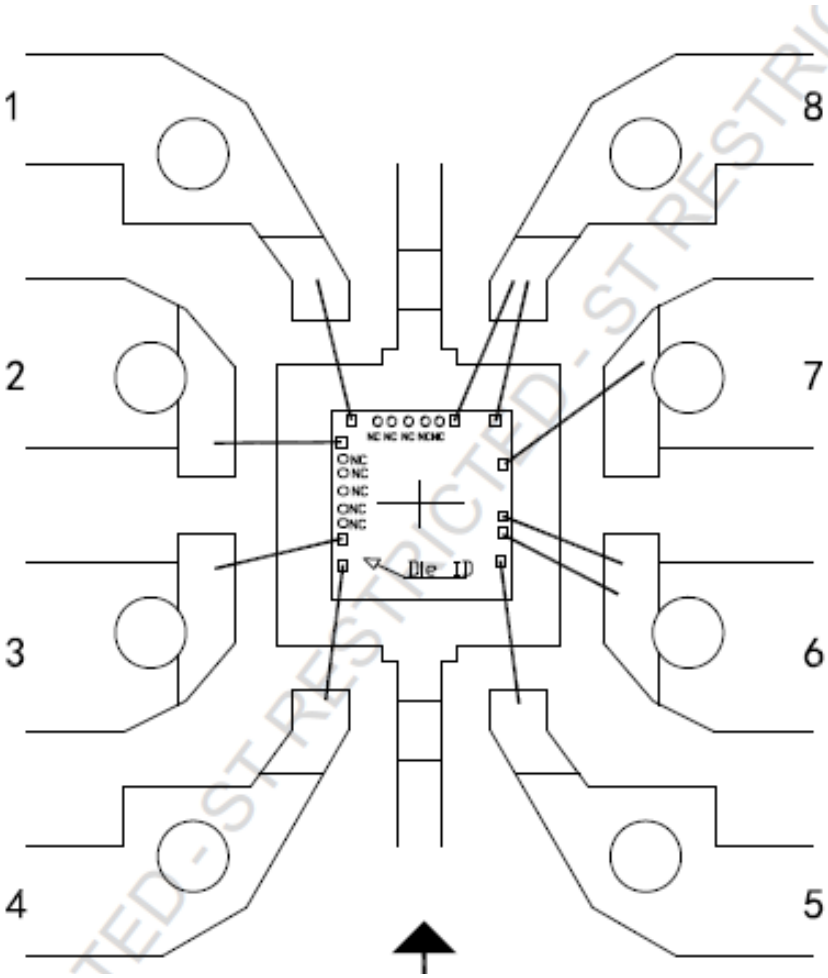


N°	Pin	Function
1	INV	Inverting input of the error amplifier. The information on the output voltage of the PFC pre-regulator is fed into the pin through a resistor divider.
2	COMP	Output of the error amplifier. A compensation network is placed between this pin and INV (pin #1) to achieve stability of the voltage control loop and ensure high power factor and low THD.
3	MULT	Main input to the multiplier. This pin is connected to the rectified mains voltage via a resistor divider and provides the sinusoidal reference to the current loop.
4	CS	Input to the PWM comparator. The current flowing in the MOSFET is sensed through a resistor, the resulting voltage is applied to this pin and compared with an internal sinusoidal-shaped reference, generated by the multiplier, to determine MOSFET's turn-off.
5	ZCD	Boost inductor's demagnetization sensing input for transition-mode operation. A negative-going edge triggers MOSFET's turn-on.
6	GND	Ground. Current return for both the signal part of the IC and the gate driver.
7	GD	Gate driver output. The totem pole output stage is able to drive power MOSFET's and IGBT's with a peak current of 600 mA source and 800 mA sink. The high-level voltage of this pin is clamped at about 12V to avoid excessive gate voltages in case the pin is supplied with a high Vcc.
8	Vcc	Supply Voltage of both the signal part of the IC and the gate driver. The supply voltage upper limit is extended to 22V min. to provide more headroom for supply voltage changes.

3.1.3 Block diagram



3.1.4 Bonding diagram

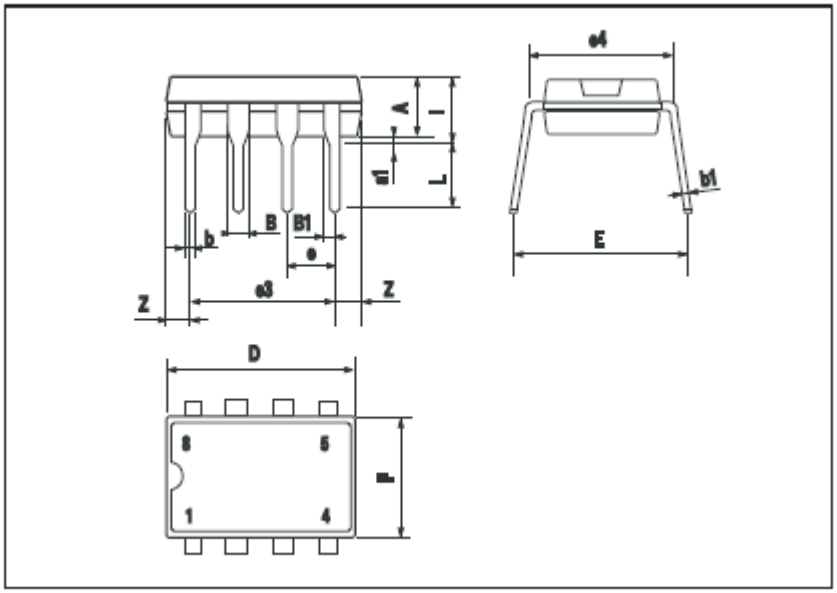


3.1.5 Package outline/Mechanical data

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A		3.32			0.131	
a1	0.51			0.020		
B	1.15		1.65	0.045		0.065
b	0.356		0.55	0.014		0.022
b1	0.204		0.304	0.008		0.012
D			10.92			0.430
E	7.95		9.75	0.313		0.384
e		2.54			0.100	
e3		7.62			0.300	
e4		7.62			0.300	
F			6.6			0.260
I			5.08			0.200
L	3.18		3.81	0.125		0.150
Z			1.52			0.060

OUTLINE AND MECHANICAL DATA

DIP-8



3.2 Traceability

Wafer fab information UE27 BD6	
Wafer fab manufacturing location	*ANG MO KIO*
Wafer diameter	*6 inches*
Wafer thickness	*375µm*
Silicon process technology	*BCD2*
Die finishing back side	*CHROMIUM/NICKEL*
Die size	*1790x1870µm*
Bond pad metallization layers	*AlSiCu*
Passivation	*Polyimide*
Metal levels	*2*

Assembly Information	
Assembly plant location	*Nantong Fujitsu - China*
Package description	*PDIP8*
Die pad size	*2.54x2.54mm*
Molding compound	*8200*
Wires bonding materials/diameters	*Cu/1mil*
Die attach material	*8390S25*
Lead solder material	*Sn*

4 TESTS RESULTS SUMMARY

4.1 Test plan and results summary

Die Oriented Tests					
Test	**Method**	**Conditions**	**Failure/SS**	**Duration**	**Note**
HTRB	High Temperature Reverse Bias				
		Tj=150°C Vdd=18V	**0/77**	**168h:0 rej 500h:0 rej 1000h: WK36**	
HTOL	High Temperature Operating Life				
		Tj=150°C Vdd=18V	**0/77**	**168h:0 rej 500h:0 rej 1000h:WK36**	

Package Oriented Tests					
Test	**Method**	**Conditions**	**Failure/SS**	**Duration**	**Note**
AC	Autoclave				
		121°C 2atm	**0/77**	**168h**	
TC	Temperature Cycling				
		Temp. range: -50/+150°C	**0/77**	**500cy:0 rej 1000cy:0 rej**	
HTSL	High Temperature Storage				
		Tamb=150°C	**0/77**	**500h:0 rej 1000h: WK36**	

5 TESTS DESCRIPTION & DETAILED RESULTS

5.1 Die oriented tests

5.1.1 High Temperature Operating Life

This test is performed like application conditions in order to check electromigration phenomena, gate oxide weakness and other design/manufacturing defects put in evidence by internal power dissipation.

The flow chart is the following:

- Initial testing @ Ta=25°C
- Check at 168 and 500hrs @ Ta=25°C
- Final Testing (1000 hr.) @ Ta=25°C

5.1.2 High Temperature Reverse Bias

This test is performed to evaluate die problems related with chip stability, layout structure, surface contamination and oxide faults.

The flow chart is the following:

- Initial testing @ Ta=25°C
- Check @ 168 and 500hrs @ Ta=25°C
- Final Testing @ 1000hrs @ Ta=25°C

5.2 Package oriented tests

5.2.1 High Temperature Storage

The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.
The scope is to investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding

5.2.2 Thermal Cycles

The purpose of this test is to evaluate the thermo mechanical behavior under moderate thermal gradient stress.
Test flow chart is the following:

- Initial testing @ Ta=25°C.
- Readout @ 500 cycles.
- Final Testing @ 1000 cycles @ Ta=25°C.

TEST CONDITIONS:

- Ta= -50°C to +150°C(air)
- 15 min. at temperature extremes
- 1 min. transfer time

5.2.3 Autoclave

The purpose of this test is to point out critical water entry path with consequent corrosion phenomena related to chemical contamination and package hermeticity.
Test flow chart is the following:

- Initial testing @ Ta=25°C.
- Final Testing (168hrs) @ Ta=25°C.

TEST CONDITIONS:

- P=2.08 atm
- Ta=121°C
- test time= 168 hrs

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