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BCM8725 PRODUCT Brief

DUAL-CHANNEL SERIAL 10-GIGABIT ETHERNET/FIBRE CHANNEL TRANSCEIVER WITH WIS LAYER AND XAUI™ INTERFACE

FEATURES

- Two fully independent channels
- Pin compatible with the BCM8724
- Integrated IEEE 802.3ae Clause 50 compliant WIS layer for EOS/WAN applications
- Support for XENPAK/X2 3.0 and XPAK MSA Optical Module standards
- Support for 10-Gigabit Fibre Channel Draft, Rev 3.0
- Support for XFP/XFI/SFP+ (SFF-8431 revision 1.1) interfaces
- Reference clock output for XFP module reference clock
- Fully integrated CMU, CDR, SerDes, Limiting Amplifier, EyeOpener®, and 4-lane XAUI™ interface
- 10-GbE PMD interface phase adjust
- XAUI link synchronization/deskew
- XAUI transmit pre-emphasis for transmission over backplanes
- PMD Transmit pre-emphasis for flexible placement of PHY
- Receive equalization on XAUI and 10-GbE serial interfaces
- Loss-of-signal detection
- Loopback modes supporting IEEE standard modes
- IEEE 802.3™ Clause 45 management interface with extended indirect address register access
- Built-in self-test (BIST) and pseudo-random bit sequence (PRBS) generator/checker
- Power dissipation: 2W
- Core Supply - 1.2V, I/O - 3.3V

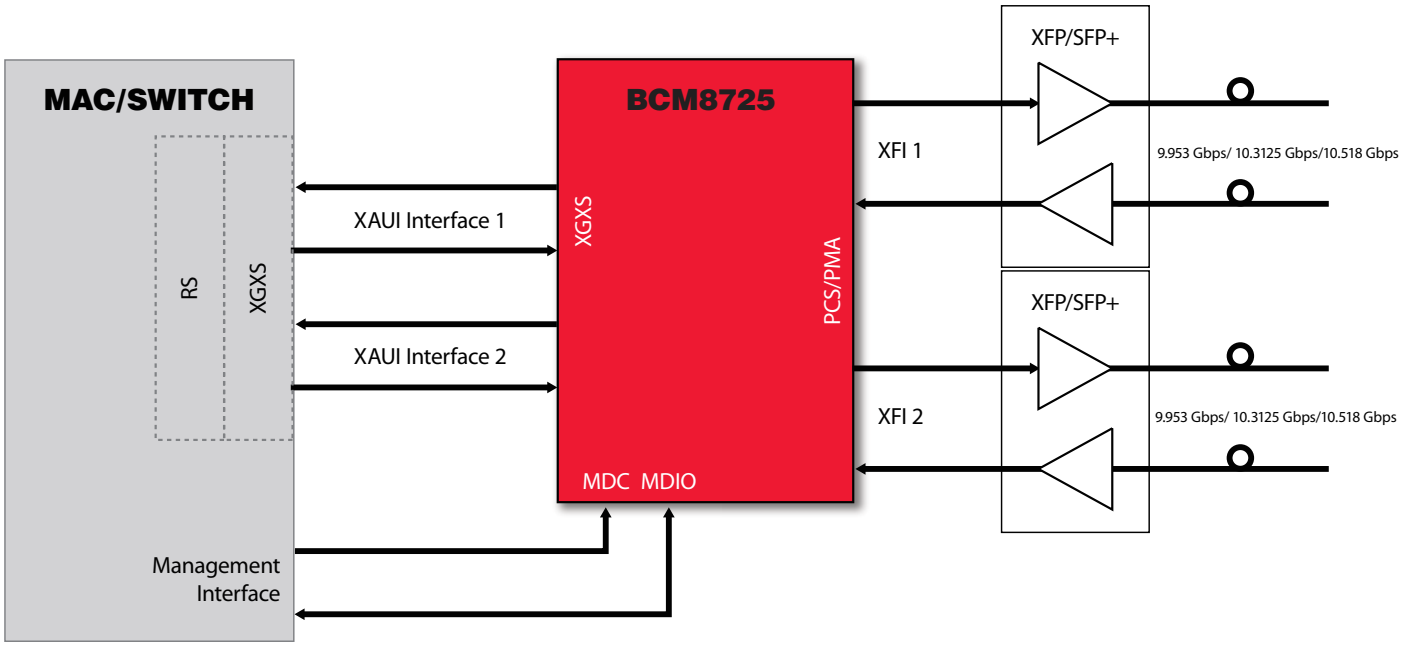
SUMMARY OF BENEFITS

- Meets or exceeds IEEE 802.3ae
- Supports XFP/XFI and SFP+ interfaces
- Simplifies designing and routing high-density line-card applications with multiple 10-GbE optical interfaces with either XFP or SFP+
- Reduces space and power in multiport 10-GbE line-card applications
- Based on a proven design that is compliant with 10-GbE interface standards
- Dual-channel LAN/WAN PHY

APPLICATIONS

- High-density 10-GbE line-cards using either SFP+ or XFP optical modules
- LAN/MAN/WAN switch/routers
- Hubs and repeaters
- Network interface cards (NICs)

OVERVIEW



BCM8725 Block Diagram

The BCM8725 Ethernet/Fibre Channel/SONET LAN/WAN PHY i s a fully integrated dual-channel serialization/deserialization (9.953 Gbps/ 10.3125 Gbps/10.5188 Gbps) interface device performing the extension functions for a 10 Gb serial Ethernet Reconciliation Sublayer (RS) interface.

For WAN applications a WIS compliant framer with flexible clocking modes allows transmission of Ethernet traffic over a WAN network. On-chip clock synthesis is performed by the high-frequency low-jitter phase-locked loops for the PMD and XAUI output retimers. Individual PMD and XAUI clock recovery is performed on the device by synchronizing directly to their respective incoming data streams. Elastic buffers are provided to allow the PMD and XAUI interfaces to operate in asynchronous configuration. Only an external 155.52 MHz/156.25 MHz/159.38 MHz oscillator is required for the reference clock input.

The BCM8725 is available in a 19 mm x 19 mm, 324-pin FBGA with 1-mm ball-pitch RoHS-compliant package.

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