181005404 Si5348 Rev D Update Rev E Release Recommended Crystal, TCXO, OCXO RM Update

PRCN Issue Date: 10/5/2018 **Effective Date:** 1/10/2019

PCN Type: Datasheet; Other; Product Revision

Description of Change

Silicon Labs is pleased to announce the following
• Update to the Recommended Crystal, TCXO, and OCXO Reference Manual for High-Performance Jitter Attenuators and Clock Generators from document revision 1.0 to revision 1.1
• Si5348 Revision D datasheet changes from document revision 1.0 to document revision 1.1
• Si5348 Revision E new product revision release and corresponding datasheet revision 0.95

After the effective date of this PCN, customers should begin using the following
• Update to the Recommended Crystal, TCXO, and OCXO Reference Manual for High-Performance Jitter Attenuators and Clock Generators from document revision 1.0 to revision 1.1
• Si5348 Revision D datasheet from document revision 1.0 to revision 1.1.
• Si5348 Revision E devices and datasheet document revision 0.95 for all new designs. The older Revision D devices will be classified as “Not Recommended for New Designs” (NRND). Currently, Silicon Labs has no plans to End of Life (EOL) the Revision D devices and will continue to support them in full production along with Revision E.

A summary of product improvements made to Si5348 Rev E over Rev D include the following:
• Lower jitter performance
• Improved hitless switching performance
• More precise phase adjust on holdover exit, startup or reset.
• PLLD supports automatic and hitless switching for up to 4 input clocks, including CMOS inputs.
• Improvements in LOS assertion
• Frequency-on-the-fly (FOTF) support added.
A detailed description of Si5348 Rev E changes can be found in application note AN1173, available on www.silabs.com. A new datasheet and reference manual have been created for Revision E. The Si5348 Revision E datasheet and reference manuals have been updated to include:
• Updated electrical specification tables with new characterization test results for Revision E
• Information added to describe new features and programming registers in Revision E
• Updated input, output, XAXB and Reference application diagrams
• Correction of typos present in the Revision D documents
• Ordering guides updated to indicate Revision E part numbers silicon

Detailed descriptions of the changes made to these documents is summarized in the change impact section of this document.

A new evaluation board is available for Si5348 Revision E device. The Revision E evaluation boards are identified as SI5348-E-EVB.

ClockBuilder Pro release 2.28.1 or later supports both Si5348 Revision D and Revision E. Customers are encouraged to download the most recent version of CBPro to take advantage of the latest software features and algorithms. A detailed description of changes for each CBPro release is available at http://www.silabs.com/Support%20Documents/Software/ClockBuilder-Pro-README.pdf.

Reason for Change

• Recommended Crystal, TCXO, and OCXO Reference Manual for High-Performance Jitter Attenuators and Clock Generators was updated to support additional Silicon Labs products, update recommended parts, and add additional information on how to select the right reference device.
• Si5348 Rev D - Updated to reflect device performance and to add additional application support information.
• Si5348 Rev E – New Rev E device improves performance and fixes errata compared to Rev D.

Impact on Form, Fit, Function, Quality, Reliability

Customers currently using Revision D in production may continue to do so. Silicon Labs will maintain production of both Revision D and Revision E concurrently.

Form:
Recommended Crystal, TCXO, and OCXO Reference Manual for High-Performance Jitter Attenuators and Clock Generators
• No changes

Si5348 Revision D
• No changes

Si5348 Revision E
The device top mark has been updated to reflect the change to Revision E. Refer to the diagram below at the end of this document. For more information, refer to the datasheet Top Marking section, located at www.silabs.com.
• Device Revision D Top Mark: First character position (R) on line 2 below is a “D”.
• Device Revision E Top Mark: First character position (R) on line 2 below is a “E”.

Fit:
Recommended Crystal, TCXO, and OCXO Reference Manual for High-Performance Jitter Attenuators and Clock Generators
• No changes

Si5348 Revision D
• No changes

Si5348 Revision E
• Si5348 Revision E device is pin-compatible and footprint-compatible with Revision D; however, Revision E devices is not intended to be drop-in replacements with Revision D. Because of changes to the circuitry in the Revision E device, its performance and behavior will not completely match that of Revision D.

Function:
Recommended Crystal, TCXO, and OCXO Reference Manual for High-Performance Jitter Attenuators and Clock Generators revision 1.1 changes
• Added Si537x/9x devices coverage.
• Added appendices explaining how to choose the right crystal and crystal oscillator for end application.
• Removed discontinued parts from recommended part tables.
• Added new parts to recommended part tables.
• Added information in recommended part tables indicating part family to make these parts easier to find on vendor website.

Si5348 Revision D document revision 1.1 September 2018 changes
• Updated Figure 3.5 Crystal Resonator Connections.
• Updated Figure 3.6 External Reference Connections.
• Updated Figure 3.8 Termination of Differential and LVCMOS Input Signals.
• Updated Figure 3.19 Supported Differential Output Termination.
• Updated Figure 3.20 LVCMOS Output Terminations.
• Updated Table 5.3 Input Clock Specifications.
• Updated Input Capacitance specification typical value.
• Updated Table 5.5 Differential Clock Output Specifications.
• Update Output-Output Skew Using Same DSPLL specification typical and max values.
• Updated Table 5.6 LVCMOS Clock Output Specifications.
• Removed Output-to-Output Skew specification.
• Updated Table 5.8 Performance Characteristics.
• Removed Input-to-Output Delay Variation specification.
• Updated Table 5.12 Crystal Specifications 1.
• Updated Table 5.14 Absolute Maximum Ratings1, 2, 3, 4.

Si5348 Revision E document revision 0.95 September 2018 release
• Si5348 Revision E devices are not intended to be a drop-in replacement with Revision D. Because of the changes made to the circuitry in the Revision E devices, its performance and behavior will not completely match that of Revision D.
• Customers that wish to migrate a design from Revision D to Revision E should download the latest version of ClockBuilder Pro and create a new custom OPN for Revision E (see application note AN1173 for more information) with their desired

configuration. Once a new Revision E OPN has been created, customers should verify functionality of the device in their system prior to starting production with Revision E.
• Silicon Labs does not recommend writing a register file, settings file or regmap that was created for Revision D to a Revision E device. When migrating an existing design from Revision D to Revision E, customers should download the latest version of ClockBuilder Pro and create new register files, settings files or regmap exports to be used with Revision E.
• Rev E has lower RMS phase jitter Typ = 95 fs, Max = 125 fs
• Rev E devices feature significantly improves hitless switching at all frequencies, including low-phase detector input frequency typically associated with low-input clock frequencies.
• Rev E devices have the option of adding a more precise phase adjust on holdover exit and can also be applied at startup or after reset. This can eliminate a phase/frequency glitch on the output clocks as they are turned on right after a power up or reset.
• Automatic switching on up to 4 input clocks to PLLD (CMOS clocks included) and hitless switching now available on CMOS clocks. Restriction of only 4 input clocks also applies to hitless switching.
• In addition to alerting on loss of signal (edge takes longer than expected), LOS can also be asserted when the period at the PFD input is smaller than expected (edge is faster than expected). This reduces the output transient when an external clock switch occurs.
• Frequency-on-the-fly (FOTF) support has been added with the Rev E. FOTF is limited to PLL A, C, D and only for PLLs with dedicated inputs (un-shared with other PLLs).
• Si5348 Rev E resolves the only identified Rev D errata: INTRb pin activity while RSTb pin held low which can be found: https://www.silabs.com/documents/public/errata/Si5348-RevD-Errata.pdf .

A detailed description of these functional changes can be found in application note AN1173, available on www.silabs.com.

Quality and Reliability:
Recommended Crystal, TCXO, and OCXO Reference Manual for High-Performance Jitter Attenuators and Clock Generators revision 1.1 changes
• No Changes

Si5348 Revision D
• No changes

Si5348 Revision E
• Qualification report and samples are available upon request for Si5348 Revision E.

Product Identification

Existing Part #	Replacement Part #	DropInCompInd.
SI5348A-D06323-GM	SI5348A-Exxxxx-GM	See Data Sheet
SI5348A-D06323-GMR	SI5348A-Exxxxx-GMR	See Data Sheet
SI5348A-D09526-GM	SI5348A-Exxxxx-GM	See Data Sheet
SI5348A-D09526-GMR	SI5348A-Exxxxx-GMR	See Data Sheet
SI5348A-D09879-GM	SI5348A-Exxxxx-GM	See Data Sheet
SI5348A-D09879-GMR	SI5348A-Exxxxx-GMR	See Data Sheet
SI5348A-D-GM	SI5348A-E-GM	See Data Sheet
SI5348A-D-GMR	SI5348A-E-GMR	See Data Sheet
SI5348B-D06789-GM	SI5348B-Exxxxx-GM	See Data Sheet
SI5348B-D06789-GMR	SI5348B-Exxxxx-GMR	See Data Sheet
SI5348B-D06827-GM	SI5348B-Exxxxx-GM	See Data Sheet
SI5348B-D06827-GMR	SI5348B-Exxxxx-GMR	See Data Sheet
SI5348B-D07011-GM	SI5348B-Exxxxx-GM	See Data Sheet
SI5348B-D07011-GMR	SI5348B-Exxxxx-GMR	See Data Sheet
SI5348B-D07570-GM	SI5348B-Exxxxx-GM	See Data Sheet
SI5348B-D07570-GMR	SI5348B-Exxxxx-GMR	See Data Sheet
SI5348B-D07993-GM	SI5348B-Exxxxx-GM	See Data Sheet
SI5348B-D07993-GMR	SI5348B-Exxxxx-GMR	See Data Sheet
SI5348B-D08008-GM	SI5348B-Exxxxx-GM	See Data Sheet
SI5348B-D08008-GMR	SI5348B-Exxxxx-GMR	See Data Sheet
SI5348B-D08033-GM	SI5348B-Exxxxx-GM	See Data Sheet
SI5348B-D08033-GMR	SI5348B-Exxxxx-GMR	See Data Sheet
SI5348B-D08034-GM	SI5348B-Exxxxx-GM	See Data Sheet
SI5348B-D08034-GMR	SI5348B-Exxxxx-GMR	See Data Sheet
SI5348B-D08039-GM	SI5348B-Exxxxx-GM	See Data Sheet
SI5348B-D08039-GMR	SI5348B-Exxxxx-GMR	See Data Sheet
SI5348B-D08040-GM	SI5348B-Exxxxx-GM	See Data Sheet
SI5348B-D08040-GMR	SI5348B-Exxxxx-GMR	See Data Sheet
SI5348B-D08142-GM	SI5348B-Exxxxx-GM	See Data Sheet
SI5348B-D08142-GMR	SI5348B-Exxxxx-GMR	See Data Sheet
SI5348B-D08231-GM	SI5348B-Exxxxx-GM	See Data Sheet
SI5348B-D08231-GMR	SI5348B-Exxxxx-GMR	See Data Sheet

SI5348B-D08557-GM	SI5348B-Exxxxx-GM	See Data Sheet
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SI5348B-D09720-GM	SI5348B-Exxxxx-GM	See Data Sheet
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SI5348B-D09733-GM	SI5348B-Exxxxx-GM	See Data Sheet
SI5348B-D09733-GMR	SI5348B-Exxxxx-GMR	See Data Sheet
SI5348B-D-GM	SI5348B-E-GM	See Data Sheet
SI5348B-D-GMR	SI5348B-E-GMR	See Data Sheet

Last Date of Unchanged Product: 1/10/2019

Qualification Samples

Available on request

Customer Response

Lack of acknowledgment of the PCN within 30 days constitutes acceptance of the change, Ref. JEDEC-J-STD-046.

To request further data or inquire about this notification, please contact your Silicon Labs sales representative. A list of Silicon Labs sales representatives is available at http://www.silabs.com.

Customers may approve early PCN acceptance by emailing approval, along with PCN # to PCNEarlyAcceptance@silabs.com

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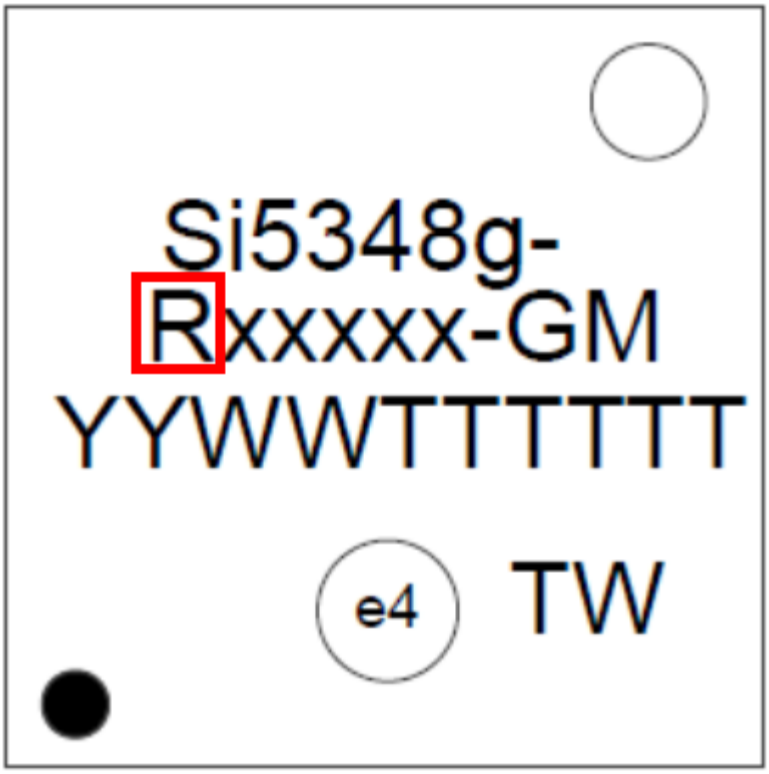
Qualification Data

Available on request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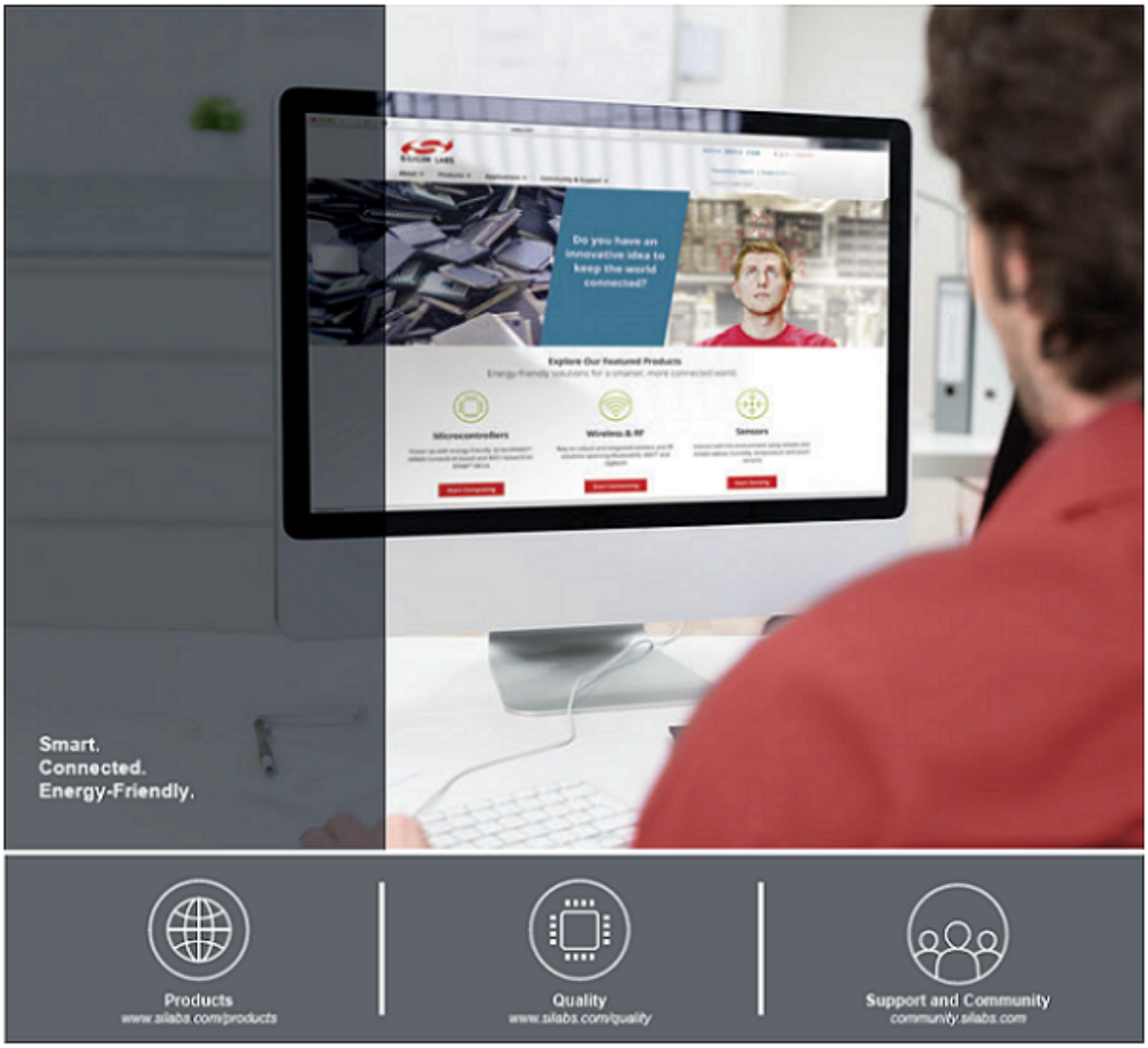

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