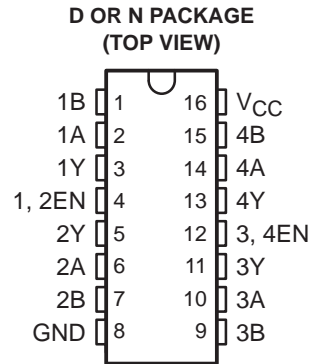


SN75ALS199 QUADRUPLE DIFFERENTIAL LINE RECEIVER

SLLS046C – JANUARY 1989 – REVISED MAY 1995

- Meets or Exceeds the Requirements of ITU Recommendations V.10, V.11, X.26, and X.27
- Designed to Operate Up To 20 Mbaud
- -7 V to 7 V Common-Mode Input Voltage Range With 300-mV Sensitivity
- 3-State TTL-Compatible Outputs
- High Input Impedance . . . 12 kΩ Min
- Input Hysteresis . . . 120 mV Typ
- Single 5-V Supply Operation
- Low Supply Current Requirement
35 mA Max
- Improved Speed and Power Consumption Compared to MC3486



description

The SN75ALS199 is a monolithic, quadruple line receiver with 3-state outputs designed using advanced, low-power, Schottky technology. This technology provides combined improvements in bar design, tooling production, and wafer fabrication, providing significantly less power consumption and permitting much higher data throughput than other designs. The device meets the specification of ITU Recommendations V.10, V.11, X.26, and X.27.

The SN75ALS199 features 3-state outputs that permit direct connection to a bus-organized system with a fail-safe design that ensures the outputs will always be high if the inputs are open. The device is optimized for balanced multipoint bus transmission at rates up to 20 megabits per second. The input features high-input impedance, input hysteresis for increased noise immunity, and an input sensitivity of ± 300 mV over a common-mode input voltage range of ± 7 V. It also features an active-high enable function for each of two receiver pairs. The SN75ALS199 is designed for optimum performance when used with the SN75ALS194 quadruple, differential line driver.

The SN75ALS199 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE
(each receiver)

| DIFFERENTIAL INPUTS A-B | EN | OUTPUT Y |
|-----------------------------|----|-------------|
| $V_{ID} \geq 0.3$ V | H | H |
| -0.3 V $< V_{ID} < 0.3$ V | H | ? |
| $V_{ID} \leq -0.3$ V | H | L |
| X | L | Z |
| Open | H | H |

H = high level, L = low level, X = irrelevant,
? = indeterminate, Z = high impedance (off)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

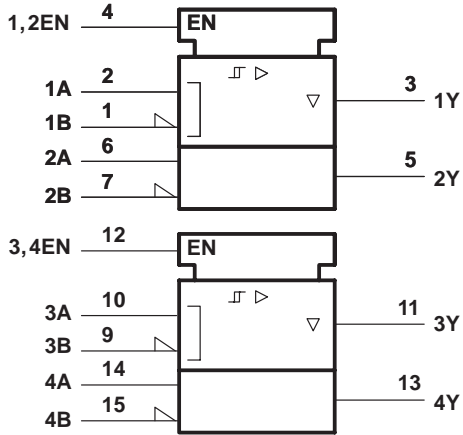
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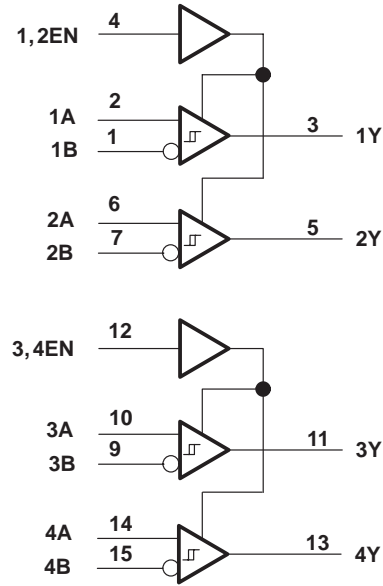
SN75ALS199 QUADRUPLE DIFFERENTIAL LINE RECEIVER

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logic symbol†

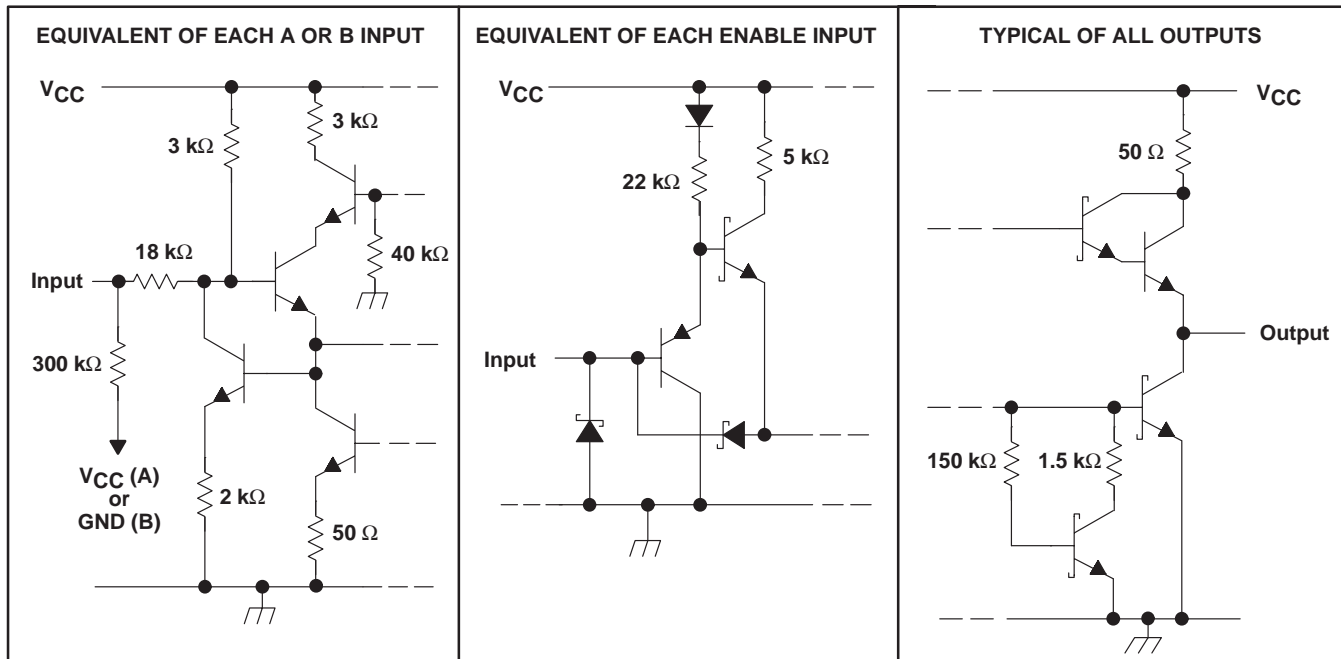


logic diagram



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

schematics of inputs and outputs



SN75ALS199 QUADRUPLE DIFFERENTIAL LINE RECEIVER

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|--|--|
| Supply voltage, V_{CC} (see Note 1) | 7 V |
| Input voltage, V_I (A or B inputs) | ± 15 V |
| Differential input voltage, V_{ID} (see Note 2) | ± 15 V |
| Enable input voltage, V_I | 7 V |
| Low-level output current, I_{OL} | 50 mA |
| Continuous total dissipation | See Dissipation Rating Table |
| Operating free-air temperature range, T_A | 0°C to 70°C |
| Storage temperature range, T_{stg} | -65°C to 150°C |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds | 260°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values, except differential input voltage, are with respect to network ground terminal.
2. Differential input voltage is measured at the noninverting input with respect to the corresponding inverting input.

DISSIPATION RATING TABLE

| PACKAGE | $T_A \leq 25^\circ\text{C}$ POWER RATING | DERATING FACTOR | $T_A = 70^\circ\text{C}$ POWER RATING |
|---------|---|--------------------------|--|
| D | 950 mW | 7.6 mW/ $^\circ\text{C}$ | 608 mW |
| N | 1150 mW | 9.2 mW/ $^\circ\text{C}$ | 736 mW |

recommended operating conditions

| | MIN | NOM | MAX | UNIT |
|---------------------------------------|------|-----|----------|------------------|
| Supply voltage, V_{CC} | 4.75 | 5 | 5.25 | V |
| Common-mode input voltage, V_{IC} | | | ± 7 | V |
| Differential input voltage, V_{ID} | | | ± 12 | V |
| High-level input voltage, V_{IH} | 2 | | | V |
| Low-level input voltage, V_{IL} | | | 0.8 | V |
| High-level output current, I_{OH} | | | -400 | μA |
| Low-level output current, I_{OL} | | | 16 | mA |
| Operating free-air temperature, T_A | 0 | | 70 | $^\circ\text{C}$ |

SN75ALS199

QUADRUPLE DIFFERENTIAL LINE RECEIVER

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electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP† | MAX | UNIT |
|--|---|--------------------------|------|------|------|
| V _{IT+} Positive-going input threshold voltage | | | | 300 | mV |
| V _{IT-} Negative-going input threshold voltage | | -300‡ | | | mV |
| V _{hys} Hysteresis voltage (V _{IT+} - V _{IT-}) | | | 120 | | mV |
| V _{IK} Enable-input clamp voltage | I _I = -18 mA | | | -1.5 | V |
| V _{OH} High-level output voltage | V _{ID} = 300 mV, I _{OH} = -400 μA | 2.7 | 3.6 | | V |
| V _{OL} Low-level output voltage | V _{ID} = -300 mV | I _{OL} = 8 mA | | 0.45 | V |
| | | I _{OL} = 16 mA | | 0.5 | |
| I _{OZ} High-impedance-state output current | V _{IL} = 0.8 V, V _{ID} = -3 V, V _O = 2.7 V | | | 20 | μA |
| | V _{IL} = 0.8 V, V _{IO} = 3 V, V _O = 0.5 V | | | -20 | |
| I _I Line input current | Other input at 0 V, See Note 3 | V _I = 15 V | 0.7 | 1.2 | mA |
| | | V _I = -15 V | -1 | -1.7 | |
| I _{IH} High-level enable-input current | | V _{IH} = 2.7 V | | 20 | μA |
| | | V _{IH} = 5.25 V | | 100 | |
| I _{IL} Low-level enable-input current | V _{IL} = 0.4 V | | | -100 | μA |
| Input resistance | | 12 | 18 | | kΩ |
| I _{OS} Short-circuit output current§ | V _{ID} = 3 V, V _O = 0 | -15 | -78 | -130 | mA |
| I _{CC} Supply current | Outputs disabled | | 22 | 35 | mA |

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ The algebraic convention, in which the less positive limit is designated minimum, is used in this data sheet for threshold voltage levels only.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

NOTE 3: Refer to ITU Recommendations V.10 and V.11 for exact conditions.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|--|-----|-----|-----|------|
| t _{PLH} Propagation delay time, low- to high-level output | V _{ID} = 0 V to 3 V, C _L = 15 pF, See Figure 2 | | 15 | 22 | ns |
| t _{PHL} Propagation delay time, high- to low-level output | | | 15 | 22 | |
| t _{PZH} Output enable time to high level | C _L = 15 pF, See Figure 3 | | 13 | 25 | ns |
| t _{PZL} Output enable time to low level | | | 11 | 25 | |
| t _{PHZ} Output disable time from high level | C _L = 15 pF, See Figure 3 | | 13 | 25 | ns |
| t _{PLZ} Output disable time from low level | | | 15 | 22 | |



PARAMETER MEASUREMENT INFORMATION

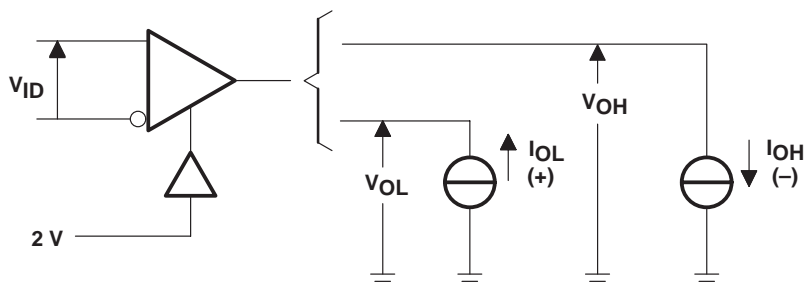
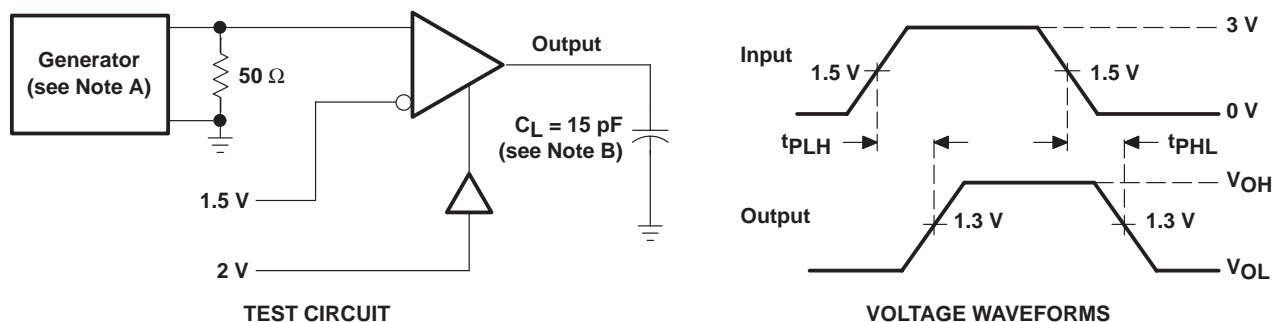


Figure 1. V_{OH} and V_{OL} Test Circuit



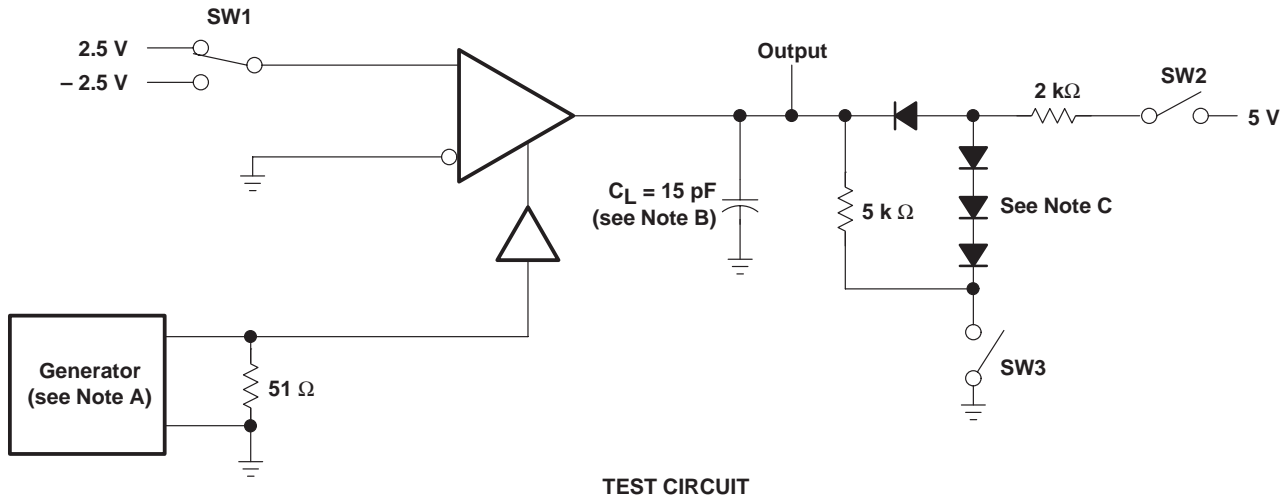
- NOTES: A. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 1$ MHz, duty cycle $\leq 50\%$, $Z_O = 50 \Omega$, $t_r \leq 6$ ns, $t_f \leq 6$ ns.
 B. C_L includes probe and jig capacitance.

Figure 2. Test Circuit and Voltage Waveforms

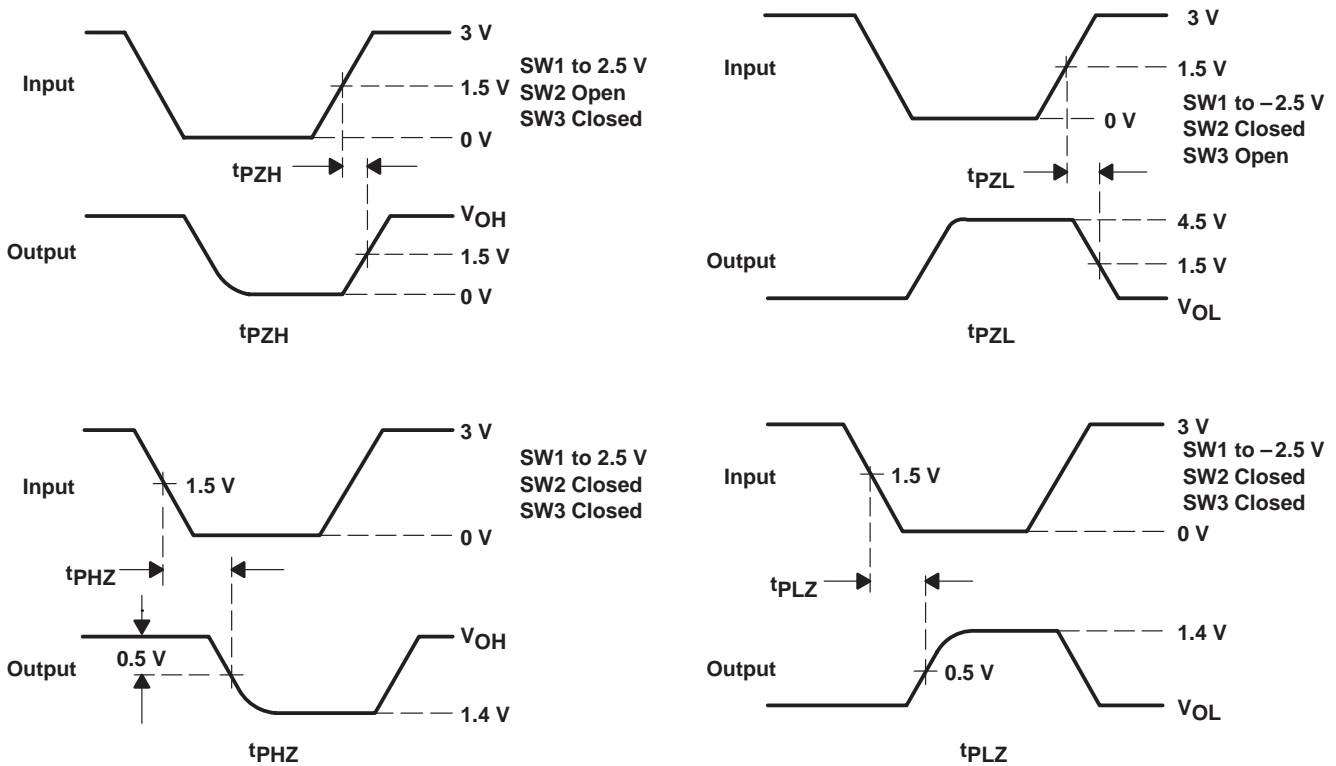
SN75ALS199 QUADRUPLE DIFFERENTIAL LINE RECEIVER

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PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

- NOTES: A. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 1 \text{ MHz}$, duty cycle $\leq 50\%$, $Z_O = 50 \Omega$, $t_r \leq 6 \text{ ns}$, $t_f \leq 6 \text{ ns}$.
 B. C_L includes probe and jig capacitance.
 C. All diodes are 1N3064 or equivalent.

Figure 3. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

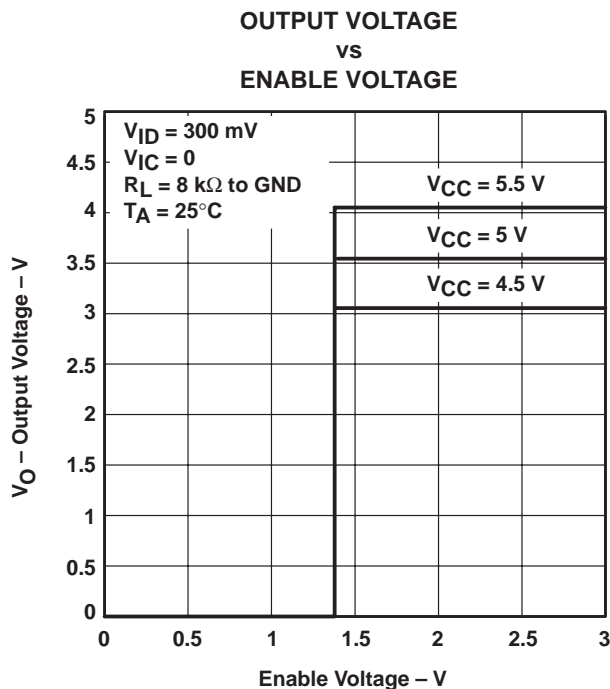


Figure 4

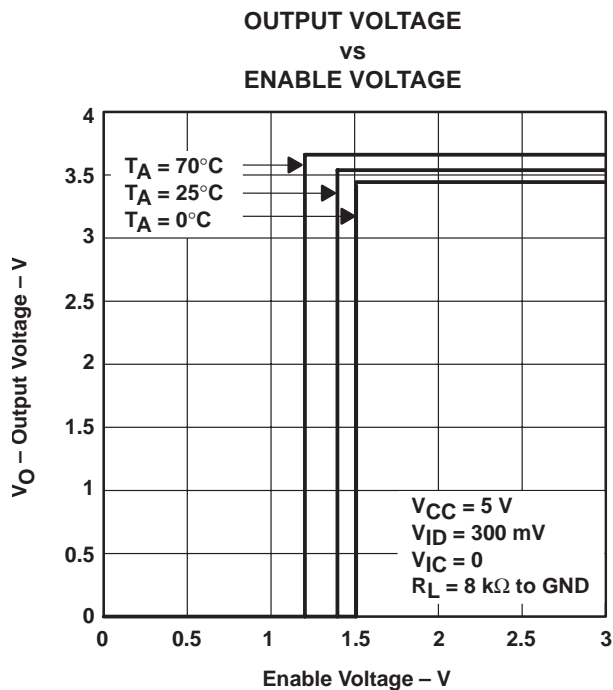


Figure 5

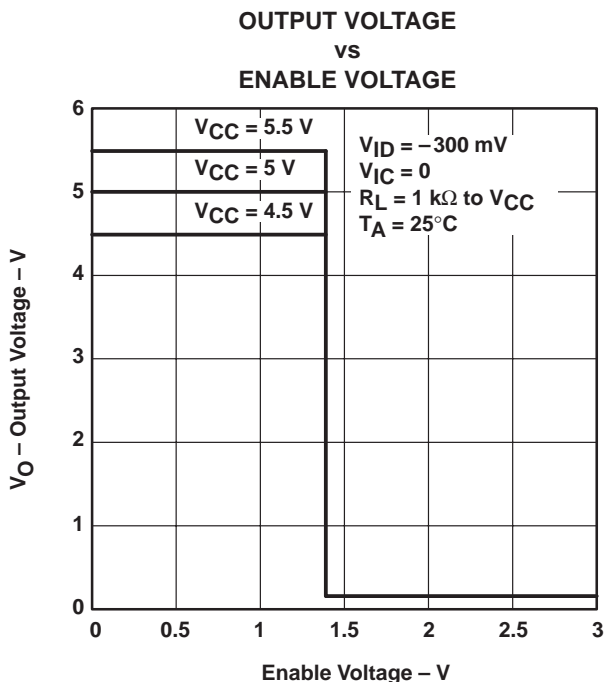


Figure 6

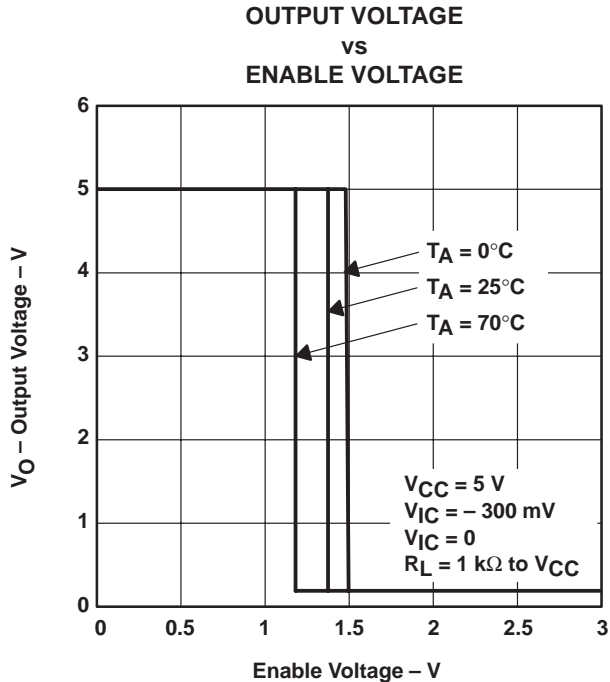


Figure 7

SN75ALS199 QUADRUPLE DIFFERENTIAL LINE RECEIVER

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TYPICAL CHARACTERISTICS

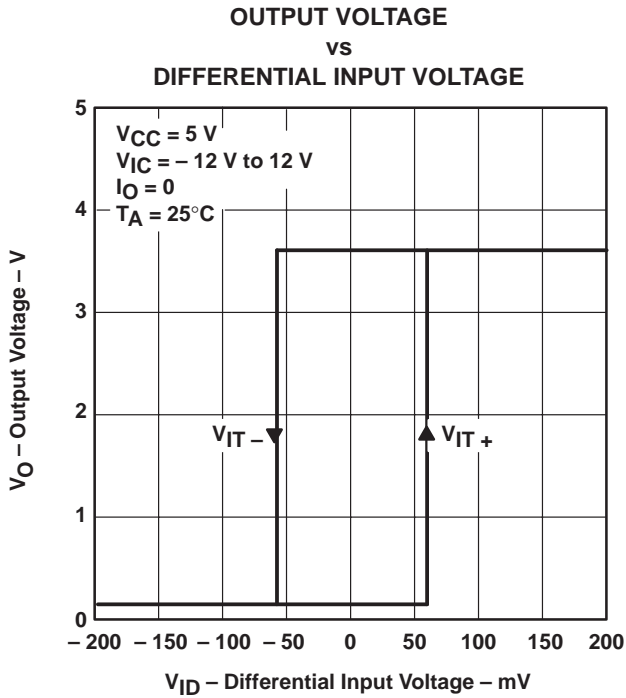


Figure 8

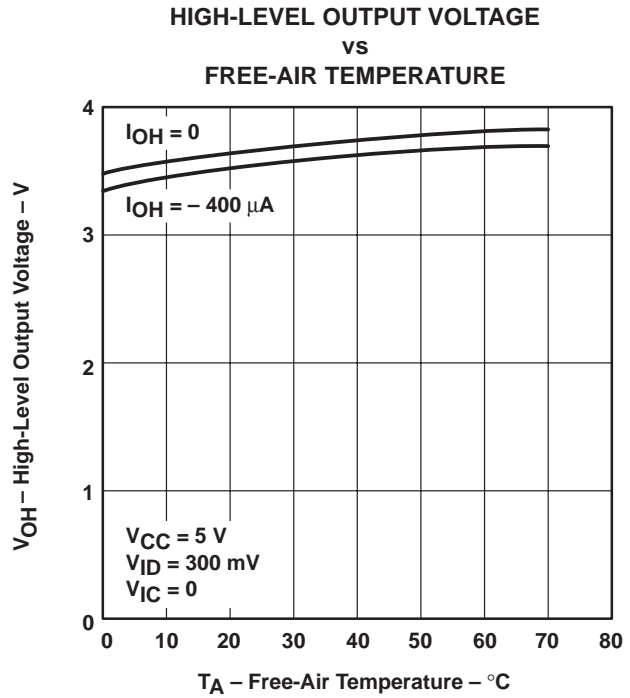


Figure 9

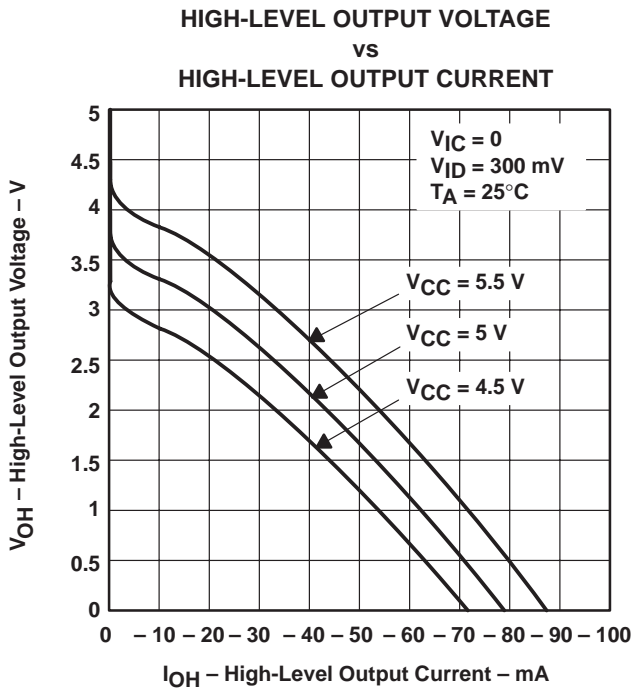


Figure 10

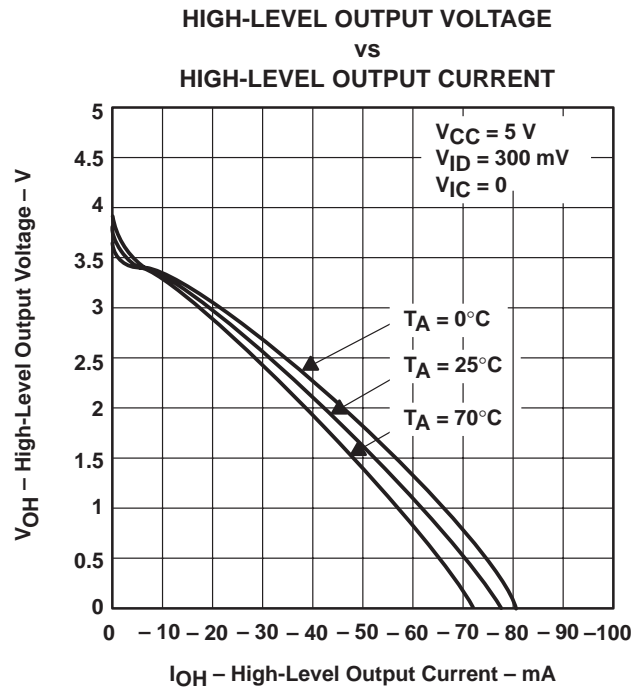


Figure 11

TYPICAL CHARACTERISTICS

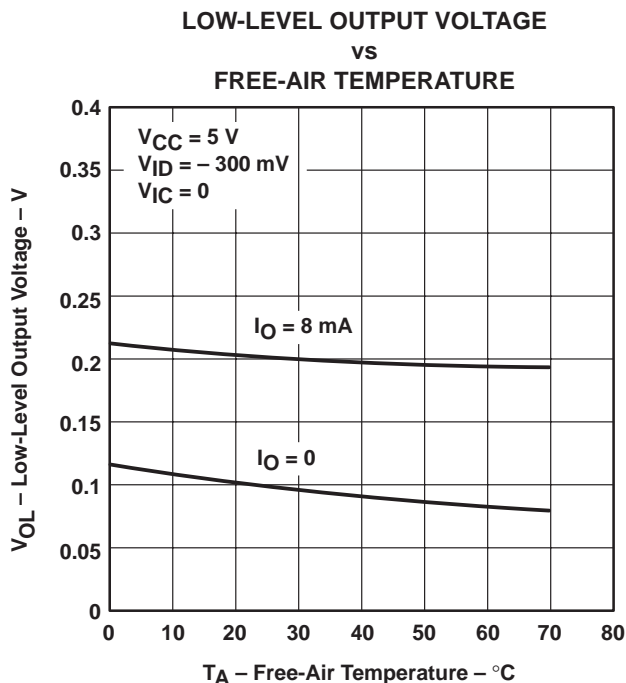


Figure 12

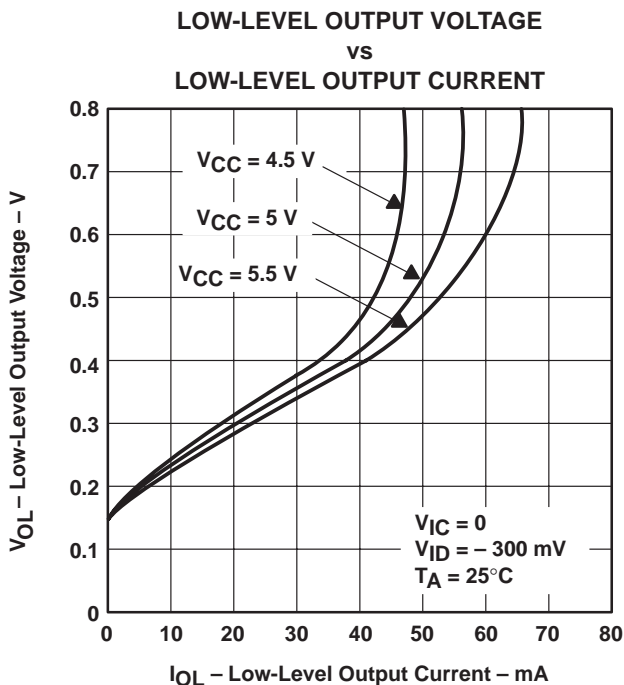


Figure 13

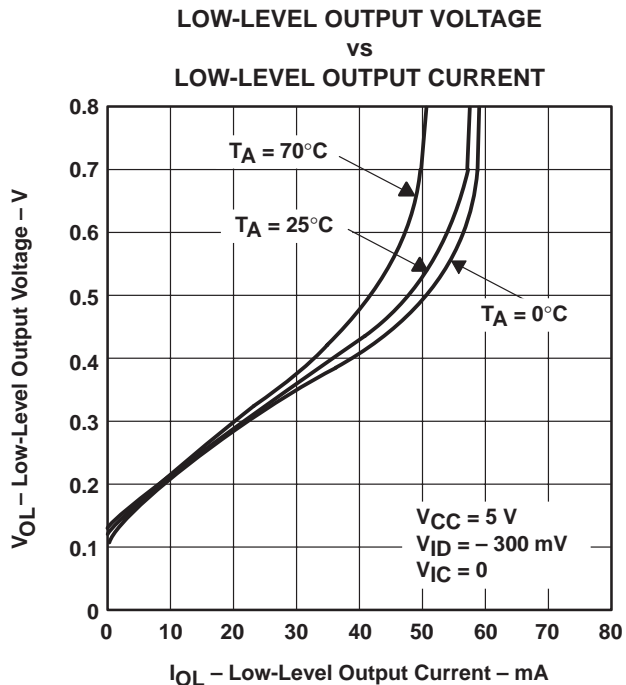


Figure 14

SN75ALS199 QUADRUPLE DIFFERENTIAL LINE RECEIVER

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TYPICAL CHARACTERISTICS

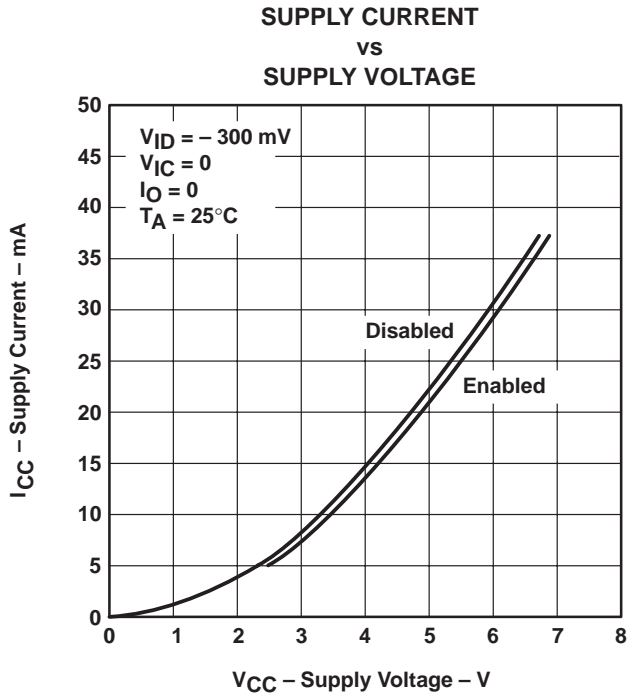


Figure 15

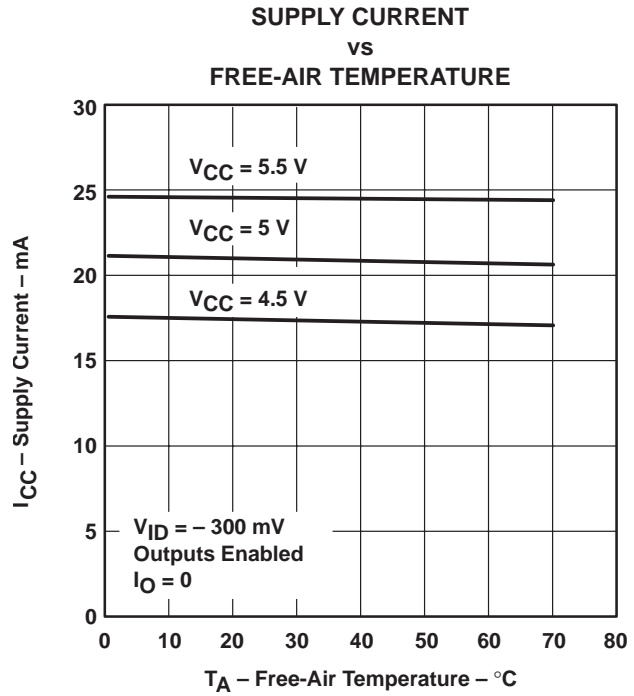


Figure 16

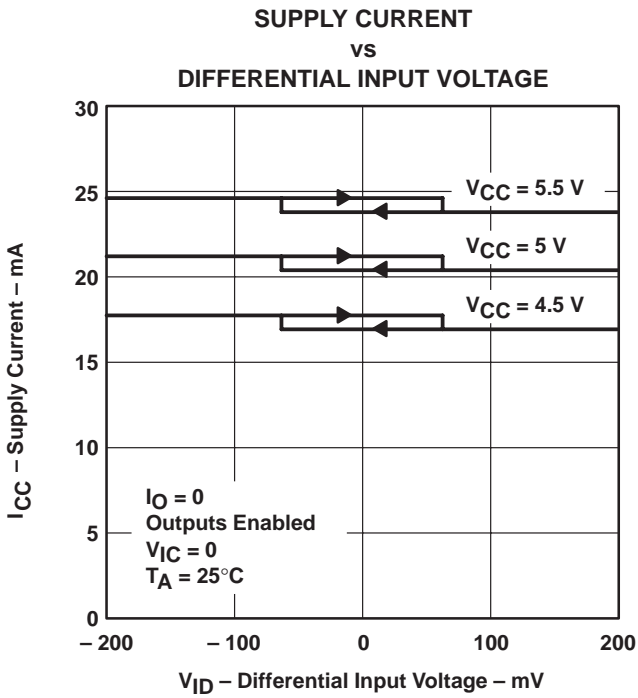


Figure 17

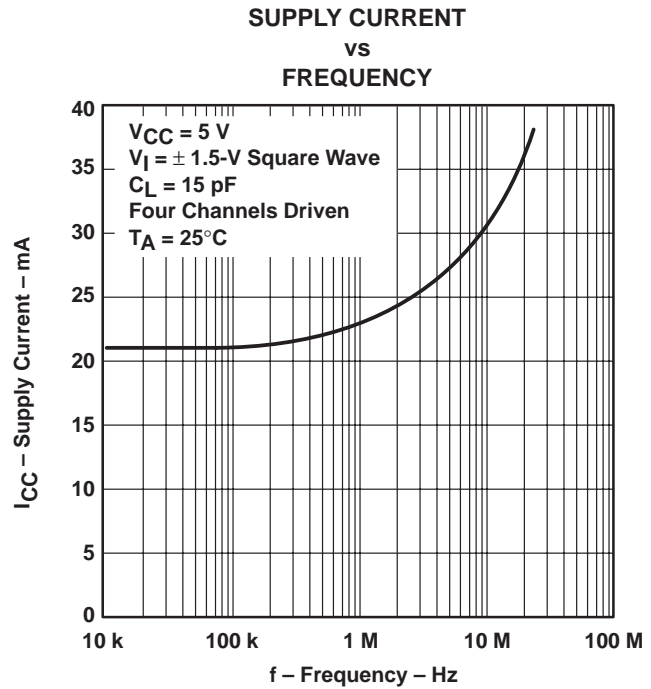


Figure 18

TYPICAL CHARACTERISTICS

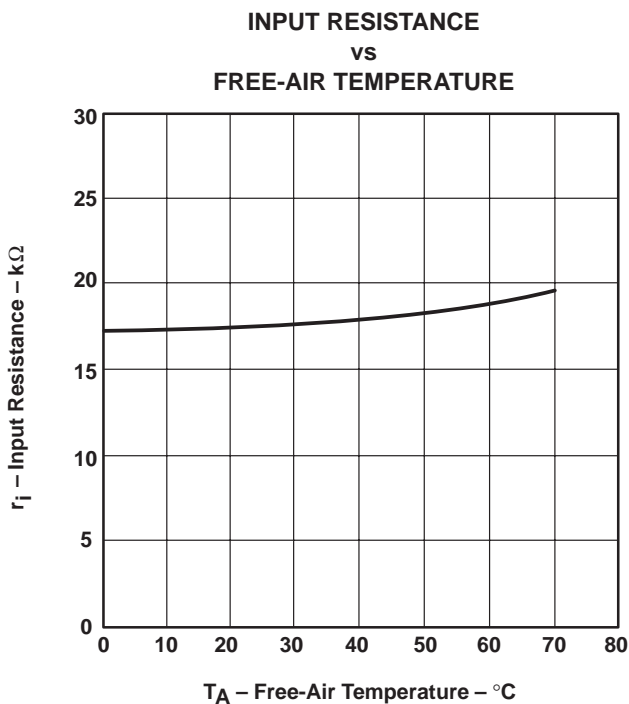


Figure 19

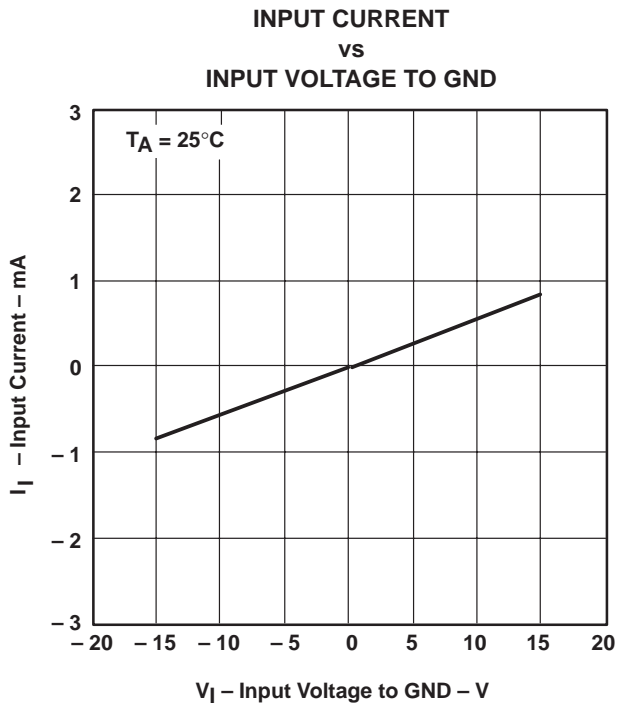


Figure 20

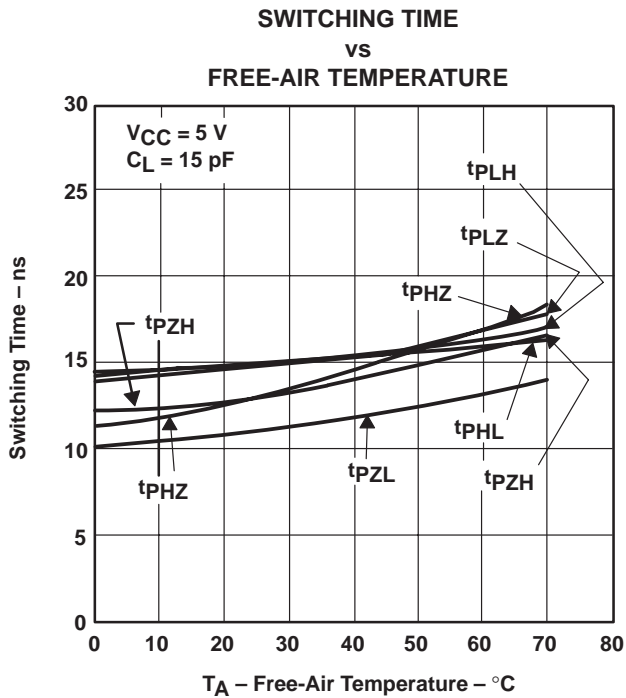


Figure 21

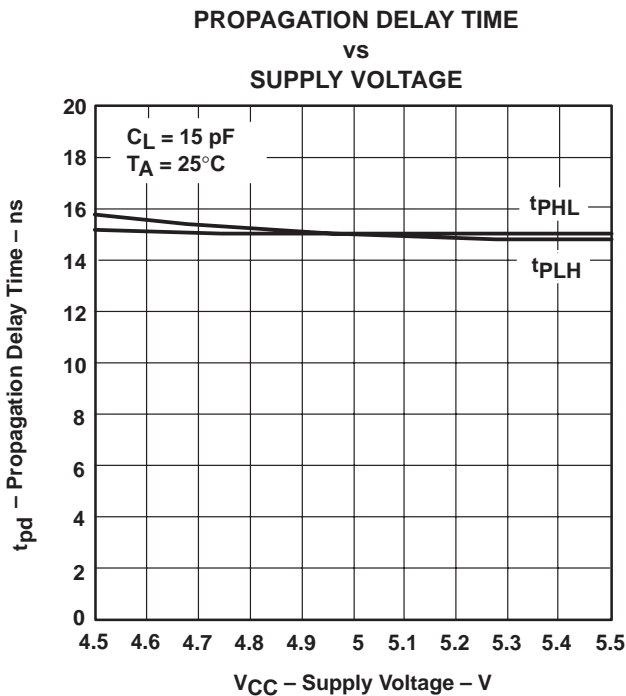


Figure 22

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| SN75ALS199D | ACTIVE | SOIC | D | 16 | 40 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 75ALS199 | Samples |
| SN75ALS199DR | ACTIVE | SOIC | D | 16 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | 75ALS199 | Samples |
| SN75ALS199N | ACTIVE | PDIP | N | 16 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | 0 to 70 | SN75ALS199N | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN75ALS199DR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS

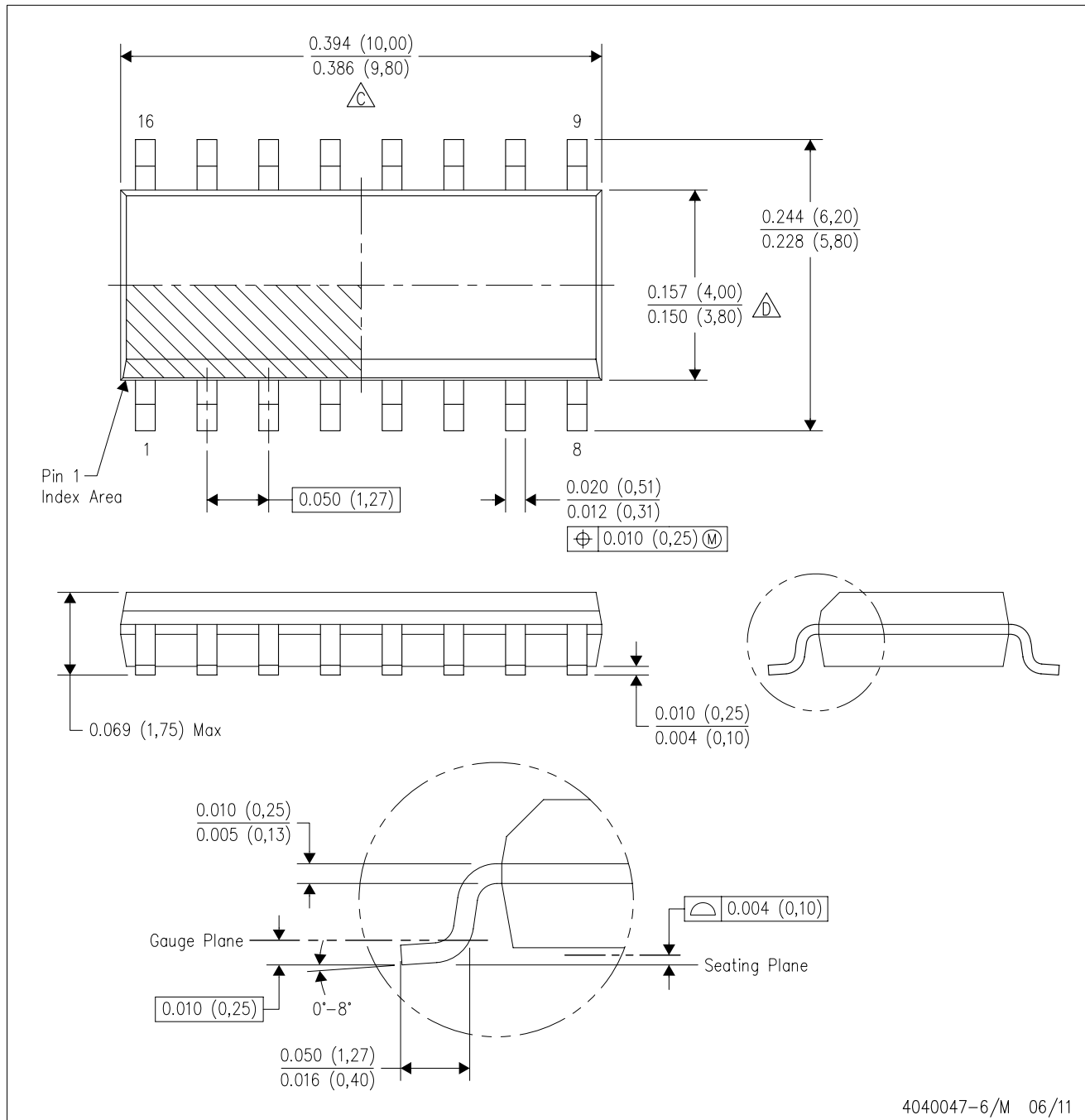


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN75ALS199DR | SOIC | D | 16 | 2500 | 333.2 | 345.9 | 28.6 |

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

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