Dear customer

LAPIS Semiconductor Co., Ltd. ("LAPIS Semiconductor"), on the 1st day of October, 2020, implemented the incorporation-type company split (shinsetsu-bunkatsu) in which LAPIS established a new company, LAPIS Technology Co., Ltd. (“LAPIS Technology”) and LAPIS Technology succeeded LAPIS Semiconductor’s LSI business.

Therefore, all references to "LAPIS Semiconductor Co., Ltd.", "LAPIS Semiconductor" and/or "LAPIS" in this document shall be replaced with "LAPIS Technology Co., Ltd."

Furthermore, there are no changes to the documents relating to our products other than the company name, the company trademark, logo, etc.

Thank you for your understanding.

LAPIS Technology Co., Ltd.
October 1, 2020

FEDL610Q101-04
Issue Date: Dec 5, 2018

ML610Q101/ML610Q102

8-bit Microcontroller

GENERAL DESCRIPTION

This LSI is a high-performance 8-bit CMOS microcontroller into which rich peripheral circuits, such as timers, PWM, UART, voltage level supervisor (VLS) function, and 10-bit successive approximation type A/D converter, are incorporated around 8-bit CPU nX-U8/100.
The CPU nX-U8/100 is capable of efficient instruction execution in 1-intruction 1-clock mode by pipe line architecture parallel processing.
The on-chip debug function that is installed enables program debugging and programming.

FEATURES

· CPU
- 8-bit RISC CPU (CPU name: nX-U8/100)
- Instruction system: 16-bit instructions
- Instruction set:
  Transfer, arithmetic operations, comparison, logic operations, multiplication/division, bit manipulations, bit logic operations, jump, conditional jump, call return stack manipulations, arithmetic shift, and so on
- On-Chip debug function
- Minimum instruction execution time
  30.5μs (@32.768kHz system clock)
  0.122μs (@8.192MHz system clock)

· Internal memory
- ML610Q101 : Internal 4Kbyte Flash ROM* (2K´ 16 bits) (including unusable 32 byte test data area)
- ML610Q102 : Internal 6Kbyte Flash ROM* (3K´ 16 bits) (including unusable 32 byte test data area)
- Internal 256byte data RAM (256´ 8 bits)

*: This product uses SuperFlash® technology licensed from Silicon Storage Technology, Inc. SuperFlash® is a registered trademark of Silicon Storage Technology, Inc.

· Interrupt controller
- 1 non-maskable interrupt source (Internal source: 1)
- 21 maskable interrupt sources (Internal sources: 16, External sources: 5)

· Time base counter (TBC)
- Low-speed time base counter ´ 1 channel
- High-speed time base counter ´ 1 channel

· Watchdog timer (WDT)
- Non-maskable interrupt and reset
- Free running
- Overflow period: 4 types selectable (125ms, 500ms, 2s, and 8s)

· Timer
- 8 bits ´ 6 channels (16-bit configuration available)
- Support Continuos mode/one shot mode
- Timer start/stop function by software or external trigger input

· PWM
- Resolution 16 bits ´ 1 channel
- Support Continuos mode/one shot mode
- PWM start/stop function by software or external trigger input

· UART
- Half-duplex
- TXD/RXD ´ 1 channels
- Bit length, parity/no parity, odd parity/even parity, 1 stop bit/2 stop bits
- Positive logic/negative logic selectable
- Built-in baud rate generator

· Successive approximation type A/D converter (SA-ADC)
- 10-bit A/D converter
- Input ´ 6 channels

· Analog Comparator
- Operating voltage: V_{DD} = 2.7V to 5.5V
- Input voltage by common mode: V_{DD} = 0.1V to V_{DD} - 1.5V
- Hysteresis (Comparator0 only): 20mV(Typ.)
- Allows selection of interrupt disabled mode,falling-edge interrupt mode,rising-edge interrupt mode, or both-edge interrupt mode.

· General-purpose ports (GPIO)
- Input/output port ´ 11 channels (including secondary functions)

· Reset
- Reset by the RESET_N pin
- Reset by power-on detection
- Reset by the watchdog timer (WDT) overflow
- Reset by voltage level supervisor(VLS)

· Voltage level supervisor(VLS)
- Judgment accuracy: ±3.0% (Typ.)
- It can be used for low level detection reset.

· Clock
- Low-speed clock:
  Built-in RC oscillation (32.768 kHz)
- High-speed clock:
  Built-in PLL oscillation (16.384 MHz), external clock
  The clock of the CPU is 8.192MHz(Max)
- Selection of high-speed clock mode by software:
  Built-in PLL oscillation, external clock

· Power management
- HALT mode: Instruction execution by CPU is suspended (peripheral circuits are in operating states).
- STOP mode: Stop of low-speed oscillation and high-speed oscillation (Operations of CPU and peripheral circuits are stopped.)
- Clock gear: The frequency of high-speed system clock can be changed by software (1/1, 1/2, 1/4, or 1/8 of the oscillation clock)
- Block Control Function: Power down (reset registers and stop clock supply) the circuits of unused peripherals.

· Shipment
  - 16-pin plastic SSOP
    ML610Q101-xxxMB (Blank product: ML610Q101-NNNMB)
    ML610Q102-xxxMB (Blank product: ML610Q102-NNNMB)

  - 16-pin plastic WQFN
    ML610Q101-xxxGD (Blank product: ML610Q101-NNNGD)
    ML610Q102-xxxGD (Blank product: ML610Q102-NNNGD)

· Guaranteed operating range
  - Operating temperature: - 40°C to 85°C
  - Operating voltage: V_{DD} = 2.7V to 5.5V

BLOCK DIAGRAM

ML610Q101 Block Diagram

Figure 1 show the block diagram of the ML610Q101.
"*" indicates secondary function, tertiary function or quaternary function of each port.

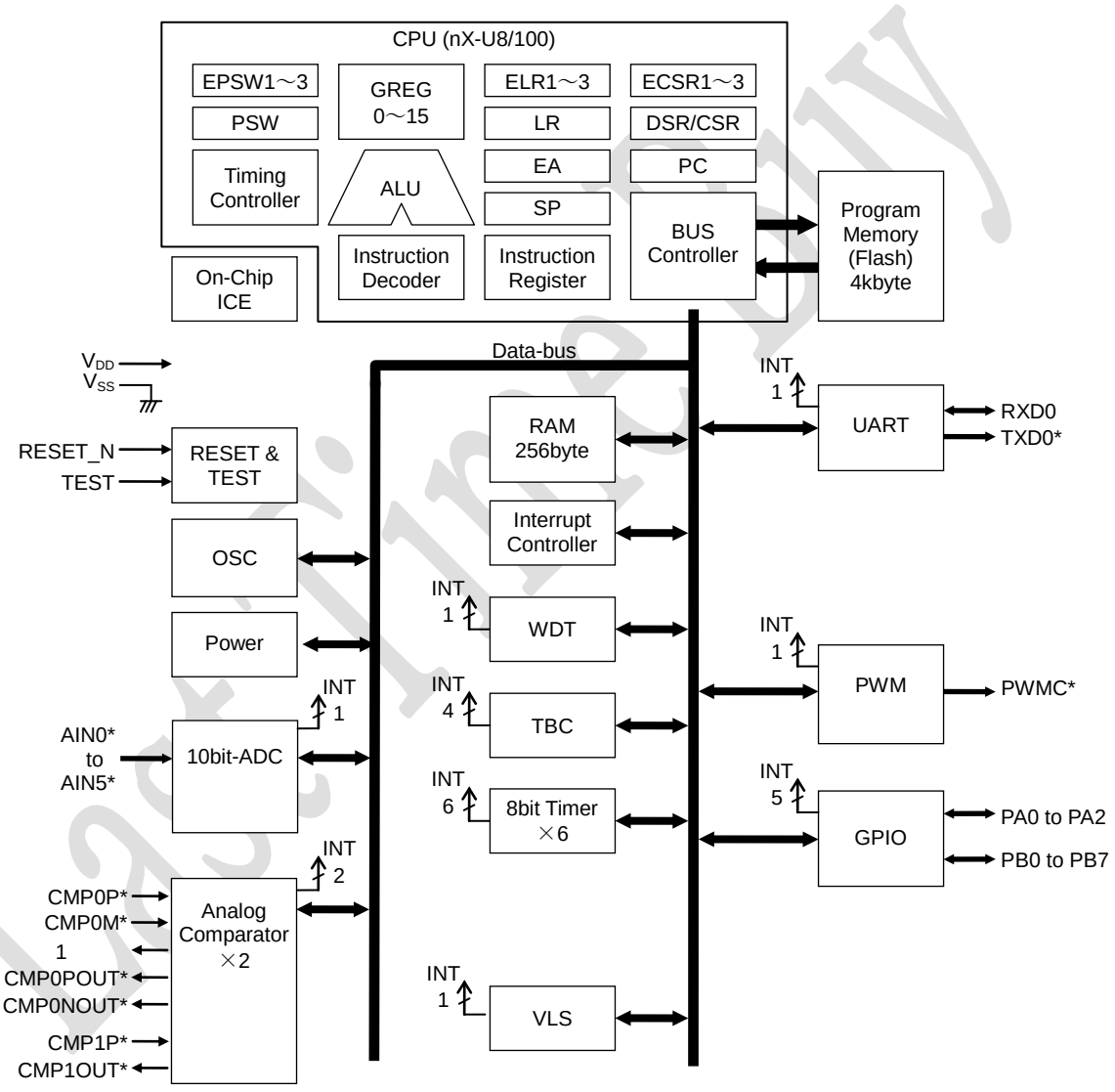


Figure 1 ML610Q101 Block Diagram

ML610Q102 Block Diagram

Figure 2 show the block diagram of the ML610Q102.
"*" indicates secondary function, tertiary function or quaternary function of each port.

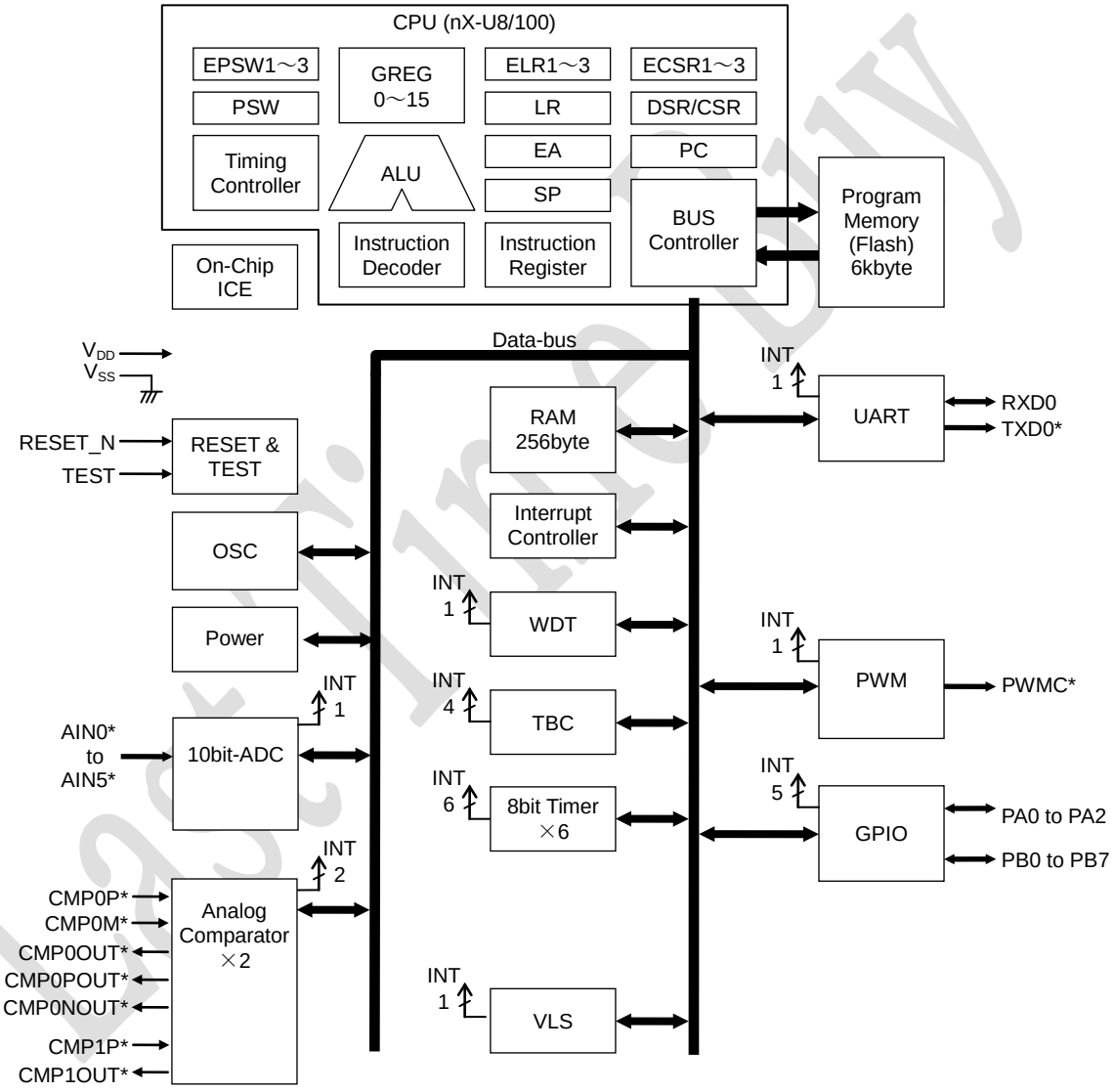


Figure 2 ML610Q102 Block Diagram

PIN CONFIGURATION

ML610Q101/ML610Q102 SSOP16 Pin Layout

Figure 3 show the SSOP16 pin layout of the ML610Q101/ML610Q102.

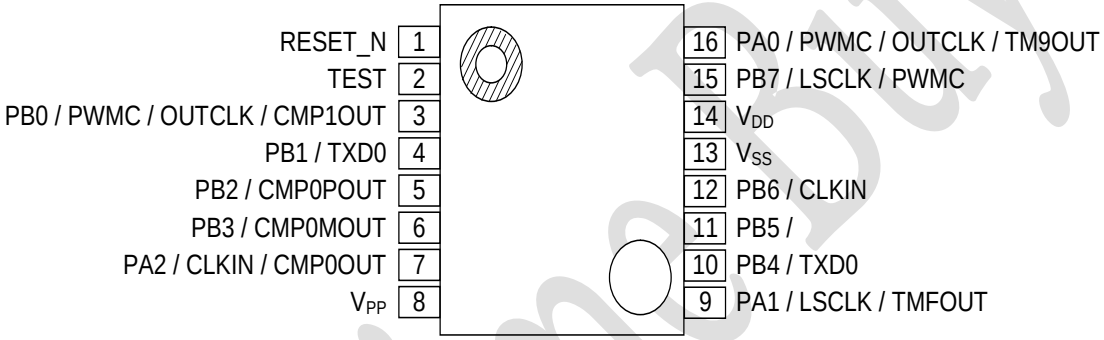


Figure 3 ML610Q101/ML610Q102 SSOP16 Pin Configuration

ML610Q101/ML610Q102 WQFN16 Pin Layout

Figure 4 show the WQFN16 pin layout of the ML610Q101/ML610Q102.

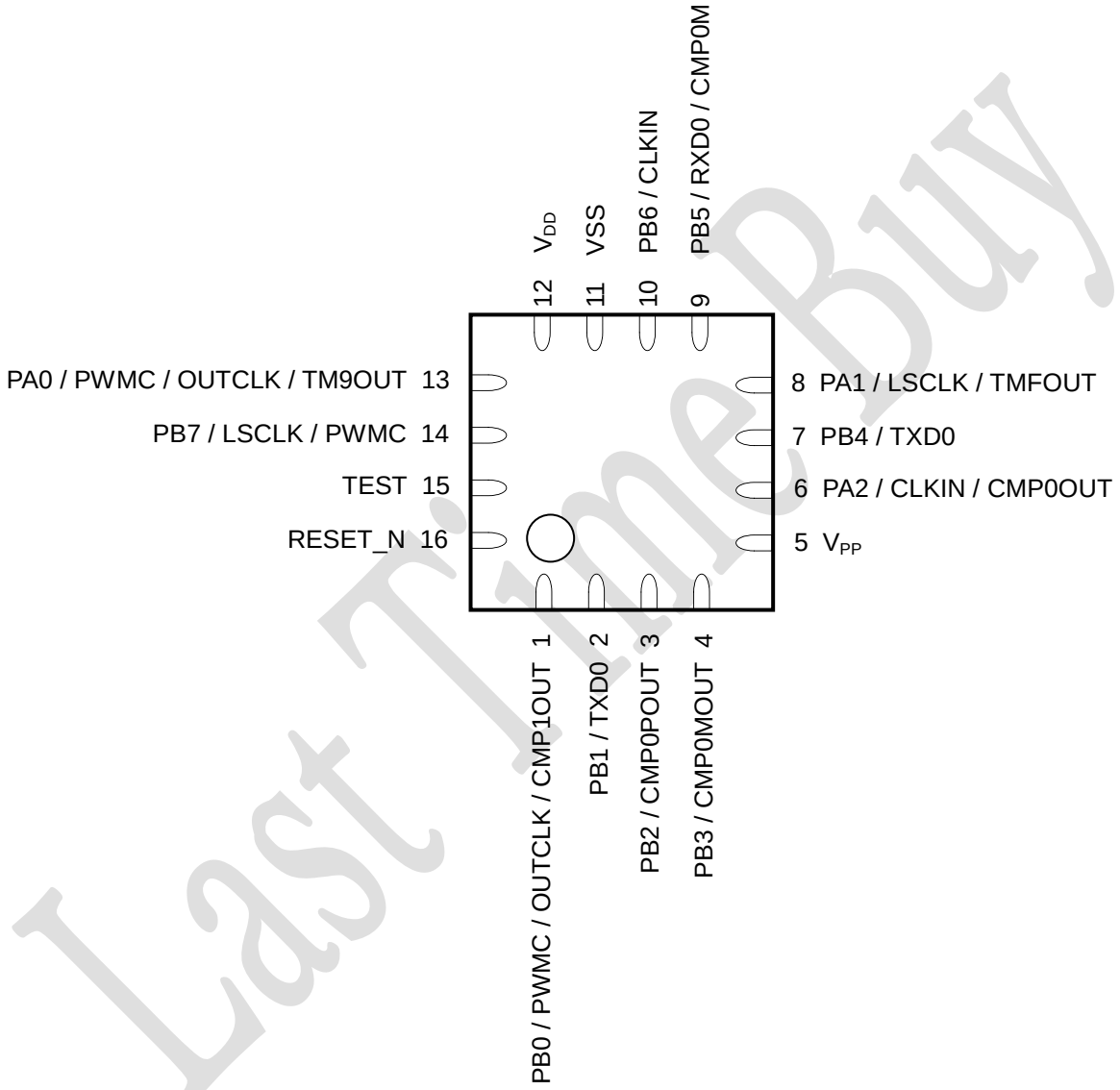


Figure 4 ML610Q101/ML610Q102 WQFN16 Pin Configuration

LIST OF PINS

PIN No. (SSOP)	PIN No. (WQFN)	Primary function			Secondary function			Tertiary function			Quaternary function		
		Pin name	I/O	Function	Pin name	I/O	Function	Pin name	I/O	Function	Pin name	I/O	Function
1	16	RESET_N	I	Reset input pin	¾	¾	¾	¾	¾	¾	¾	¾	¾
2	15	TEST	I/O	Input/output pin for testing	¾	¾	¾	¾	¾	¾	¾	¾	¾
3	1	PB0/ EXI4/ AIN2/ RXD0	I/O	Input/output port, External interrupt 4, ADC input 2, UART receive	PWMC	O	PWMC output	OUTCLK	O	High-speed clock output	CMP1 OUT	O	CMP1 output
4	2	PB1/ EXI5/ AIN3	I/O	Input/output port, External interrupt 5, ADC input 3	¾	¾	¾	TXD0	O	UART data output	¾	¾	¾
5	3	PB2	I/O	Input/output port,	¾	¾	¾	¾	¾	¾	CMP0 POUT	O	CMP0_N output
6	4	PB3	I/O	Input/output port	¾	¾	¾	¾	¾	¾	CMP0 NOUT	O	CMP0_N output
7	6	PA2/EXI2	I/O	Input/output port, External interrupt2	¾	¾	¾	CLKIN	I	clock input	CMP0 OUT	O	CMP0 output
8	5	V_{PP}	¾	Power supply pin for Flash ROM	¾	¾	¾	¾	¾	¾	¾	¾	¾
9	8	PA1/ EXI1/ AIN1/ CMP1P	I/O	Input/output port, External interrupt 1, ADC input 1, Comparator1 non-inverting input	¾	¾	¾	LSCLK	O	Low speed clock output	TMF OUT	O	timer F output
10	7	PB4/ CMP0P	I/O	Input/output port, Comparator0 non-inverting input	¾	¾	¾	TXD0	O	UART data output	¾	¾	¾
11	9	PB5/ RXD0/ CMP0M	I/O	Input/output port, UART data receive, Comparator1-inverting input	¾	¾	¾	¾	¾	¾	¾	¾	¾
12	10	PB6/ AIN4	I/O	Input/output port, ADC input 4	CLKIN	I	clock input	¾	¾	¾	¾	¾	¾
13	11	Vss	¾	Negative power supply pin	¾	¾	¾	¾	¾	¾	¾	¾	¾
14	12	V_{DD}	¾	Positive power supply pin	¾	¾	¾	¾	¾	¾	¾	¾	¾
15	14	PB7/ AIN5	I/O	Input/output port, ADC input 5	LSCLK	O	Low-speed clock output	¾	¾	¾	PWMC	O	PWMC output
16	13	PA0/ EXI0/ AIN0	I/O	Input/output port, External interrupt 0, ADC input 0	PWMC	O	PWMC output	OUTCLK	O	High-speed clock output	TM9OUT	O	timer 9 output

PIN DESCRIPTION

Pin name	I/O	Description	Primary/ Secondary/ Tertiary/ Quaternary	Logic
System				
RESET_N	I	Reset input pin. When this pin is set to a “L” level, system reset mode is set and the internal section is initialized. When this pin is set to a “H” level subsequently, program execution starts. A pull-up resistor is internally connected.	—	Negative
CLKIN	I	High-speed clock output pin. This pin is used as the tertiary function of the PA2 or the secondary function of PB6 pin.	Secondary/ Tertiary	—
LSCLK	O	Low-speed clock output pin. This pin is used as the tertiary function of the PA1 or the secondary function of the PB7 pin.	Secondary/ Tertiary	—
OUTCLK	O	High-speed clock output pin. This pin is used as the tertiary function of the PA0 or PB0 pin.	Tertiary	—
General-purpose input/output port				
PA0 to PA2 PB0 to PB7	I/O	General-purpose input/output port. Since these pins have secondary functions and tertiary functions and quaternary functions, the pins cannot be used as a port when the secondary functions and tertiary functions and quaternary functions are used.	Primary	Positive
UART				
TXD0	O	UART0 data output pin. This pin is used as the tertiary function of the PB1 or PB4 pin.	Tertiary	Positive
RXD0	I	UART0 data input pin. This pin is used as the primary function of the PB0 or PB5 or the quaternary function of the PB7 pin.	Primary	Positive
PWM				
PWMC	O	PWMC output pin. This pin is used as the secondary function of the PB0 or PA0 or the quaternary function of the PB7 pin.	Secondary Quaternary	Positive
External interrupt				
EXI0 to 2	I	External maskable interrupt input pins. Interrupt enable and edge selection can be performed for each bit by software. These pins are used as the primary functions of the PA0 – PA2 pins.	Primary	Positive/ negative
EXI4,5	I	External maskable interrupt input pins. Interrupt enable and edge selection can be performed for each bit by software. These pins are used as the primary functions of the PB0, PB1 pins.	Primary	Positive/ negative
Timer				
TnTG	I	External clock input pin used for both Timer E and Timer F.These pins are used as the primary function of the PA0-PA2, PB0-PB7 pins.	Primary	—
TM9OUT	O	Timer 9 output pin. This pin is used as the quaternary function of the PA0 pin.	Quaternary	Positive
TMFOUT	O	Timer F output pin. This pin is used as the quaternary function of the PA1 pin.	Quaternary	Positive

Pin name	I/O	Description	Primary/ Secondary/ Tertiary/ Quaternary	Logic
Successive approximation type A/D converter				
AIN0	I	Channel 0 analog input for successive approximation type A/D converter. This pin is used as the primary function of the PA0 pin.	Primary	—
AIN1	I	Channel 1 analog input for successive approximation type A/D converter. This pin is used as the primary function of the PA1 pin.	Primary	—
AIN2	I	Channel 2 analog input for successive approximation type A/D converter. This pin is used as the primary function of the PB0 pin.	Primary	—
AIN3	I	Channel 3 analog input for successive approximation type A/D converter. This pin is used as the primary function of the PB1 pin.	Primary	—
AIN4	I	Channel 4 analog input for successive approximation type A/D converter. This pin is used as the primary function of the PB6 pin.	Primary	—
AIN5	I	Channel 5 analog input for successive approximation type A/D converter. This pin is used as the primary function of the PB7 pin.	Primary	—
Conparator				
CMP0P	I	Non-inverting input for comparator0. This pin is used as the primary function of the PB4 pin.	Primary	—
CMP0M	I	Inverting input for comparator0. This pin is used as the primary function of the PB5 pin.	Primary	—
CMP0OUT	O	Output for comparator0. This pin is used as the quaternary function of the PA2 pin.	Quaternary	—
CMP0OUT	O	Output for comparator0. This pin is used as the quaternary function of the PB2 pin.	Quaternary	—
CMP0OUT	O	Output for comparator0. This pin is used as the quaternary function of the PB3 pin.	Quaternary	—
CMP1P	I	Non-inverting input for comparator1. This pin is used as the primary function of the PA1 pin.	Primary	—
CMP1OUT	O	Output for comparator1. This pin is used as the quaternary function of the PB0 pin.	Quaternary	—
For testing				
TEST	I/O	Input/output pin for testing. A pull-down resistor is internally connected.	—	Positive
Power supply				
V_{SS}	—	Negative power supply pin.	—	—
V_{DD}	—	Positive power supply pin.	—	—
V_{PP}	—	Power supply pin for Flash ROM	—	—

ML610Q101/ML610Q102 TERMINATION OF UNUSED PINS

Table 3 shows methods of terminating the unused pins for ML610Q101/ML610Q102.

Table 3 Termination of Unused Pins

Pin	Recommended pin termination
RESET_N	Open
TEST	Open
PA0 to PA2	Open
PB0 to PB7	Open
V_{PP}	Open

Note:
It is recommended to set the unused input ports and input/output ports to the inputs with pull-down resistors/pull-up resistors or the output mode since the supply current may become excessively large if the pins are left open in the high impedance input setting.

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

(V_{SS} = 0V)

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage 1	V_{DD}	Ta = 25°C	- 0.3 to +7.0	V
Power supply voltage 2	V_{PP}	Ta = 25°C	- 0.3 to +9.5	V
Input voltage	V_{IN}	Ta = 25°C	- 0.3 to V_{DD}+0.3	V
Output voltage	V_{OUT}	Ta = 25°C	- 0.3 to V_{DD}+0.3	V
Output current 1	I_{OUT1}	Ta = 25°C	- 12 to +11	mA
Power dissipation	PD	Ta = 25°C	0.5	mW
Storage temperature	T_{STG}	¾	- 55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

(V_{SS} = 0V)

Parameter	Symbol	Condition	Range	Unit
Operating temperature	T_{OP}	¾	- 40 to +85	°C
Operating voltage	V_{DD}	¾	2.7 to 5.5	V
Operating frequency (CPU)	f_{OP}	V_{DD} = 2.7V to 5.5V	30k to 8.4M	Hz

OPERATING CONDITIONS OF FLASH MEMORY

(V_{SS}=0V)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Operating temperature	T_{OP}	At write/erase	0	—	+40	°C
Operating voltage	V_{DD}	At write/erase	4.5	—	5.5	V
	V_{PP}*1	At write/erase	7.7	—	8.3	
Rewrite counts	C_{EP}	—	—	—	80	cycles
Data retention*2	Y_{DR}	—	10	—	—	years

*1 : Vpp pin has an internal pull-down resistor.

*2 : One rewrite cycle has one time erase and one time write, it counts one time even if the erase is aborted.

DC CHARACTERISTICS (1/4)

(V_{DD}=2.7 to 5.5V, V_{SS}=0V, Ta=- 40 to +85°C, unless otherwise specified)

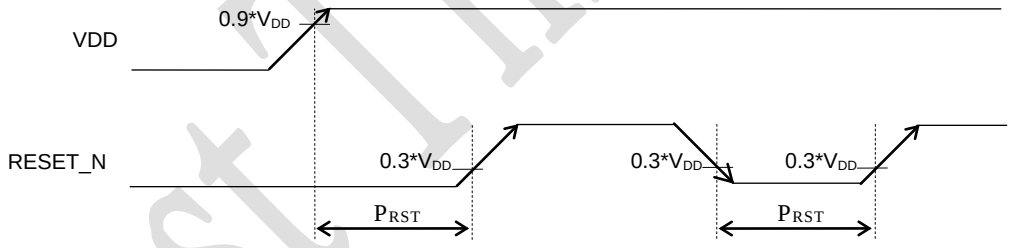
Parameter	Symbol	Condition	Rating			Unit	Measuring circuit
			Min.	Typ.	Max.		
Low-speed RC oscillation frequency	f_{RCL}	Ta = 25°C	31	32.768	34	kHz	1
PLL oscillation frequency*1*2	f_{PLL}	Ta = 25°C	Typ. - 1%	16.384	Typ. +1%	MHz	
		Ta = -10 to +85°C	Typ. -2%	16.384	Typ. +2%		
		Ta = - 40 to +85°C	Typ. - 2.5%	16.384	Typ. +2.5%		
Reset*3 pulse width	T_{RST}	¾	100	—	—	ms	
Reset*3 noise elimination pulse width	T_{NRST}	¾	—	—	0.4		
Power-on reset activation power rise time	T_{POR}	¾	—	—	10	ms	

*1 : 2048 clock average. Maximum CPU clock frequency is fPLL/2.

*2 : Guaranteed value at the factory shipment.

*3 : Reset via RESET_N pin

RESET



RESET_N pin reset

Power on reset

DC CHARACTERISTICS (2/4)

(V_{DD}=2.7 to 5.5V, V_{SS}=0V, Ta=- 40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition		Rating Min.	Rating Typ.	Rating Max.	Unit	Measuring circuit
VLS Judgment voltage	V_{VLS0F}	Ta=25°C , V_{DD}=fall		Typ - 3.0 %	2.85	Typ +3.0 %	V	1
		V_{DD}=fall		Typ. - 5.0 %	2.85	Typ. +5.0 %		
	V_{VLS0R}	Ta=25°C , V_{DD}=rise		Typ. - 3.0 %	2.92	Typ. +3.0 %		
		V_{DD}=rise		Typ. - 5.0 %	2.92	Typ. +5.0 %		
	V_{VLS1}	Ta=25°C	VLS0=0	Typ - 3.0 %	3.295	Typ +3.0 %		
			VLS0=1		3.625			
		—	VLS0=0	Typ - 5.0 %	3.295	Typ +5.0 %		
			VLS0=1		3.625			
Comparator0 In-phase input voltage range	V_{CMR}	—		0.1	—	V_{DD} -1.5	V	4
Comparator0 hysteresis	V_{HYSP}	Ta=25°C , V_{DD} = 5.0V		10	20	30	mV	
		V_{DD} = 5.0V		5	20	35		
Comparator0 Input offset voltage	V_{CMOF}	Ta=25°C , V_{DD} = 5.0V		—	—	7		
Comparator Reference-voltage error*3	V_{CMREF}	Ta=25°C		-25	—	25		
		—		-50	—	50		
Supply current 1	IDD1	CPU: In STOP state. Low-speed/high-speed oscillation: stopped.	Ta=-40 to +85°C	—	1	30	mA	1
Supply current 2	IDD2	CPU: In 32.768kHz operating state.*1 High-speed oscillation: Stopped.	Ta=-40 to +85°C	—	3.7	6	mA	

*1 : LTBC and WDT are operating ,and significant bits of BLKCON0 to BLKCON4 registers are all “1”.

*2 : When the CPU operating rate is 100%. Minimum instruction execution time: Approx 0.122 µs (at 8.192MHz system clock)

*3 :Comparator input offset voltage is included.

DC CHARACTERISTICS (3/4)

(V_{DD}=2.7 to 5.5V, V_{SS}=0V, Ta=- 40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit	Measuring circuit
			Min.	Typ.	Max.		
Output voltage	VOH	IOH1 = - 3.0mA, V_{DD} = 4.5V *1	V_{DD} - 0.7	—	—	V	2
	VOL	IOL1 = +8.5mA, V_{DD} = 4.5V *1	—	—	0.6		
Output leakage	IOOH	VOH = V_{DD} (in high-impedance state)	—	—	+1	mA	3
	IOOL	VOL = V_{SS} (in high-impedance state)	- 1	—	—		
Input current 1 (RESET_N)	IIH1	VIH1 = V_{DD}	—	—	1	mA	4
	IIL1	VIL1 = V_{SS}, V_{DD} = 5.0V	- 650	- 500	- 350		
Input current 1 (TEST)	IIH1	VIH1 = V_{DD} = 5.0V	20	115	200		
	IIL1	VIL1 = V_{SS}	- 1	—	—		
Input current 2 (PA0-PA2) (PB0-PB7)	IIH2	VIH2 = V_{DD} = 5.0V (when pulled-down)	20	115	200		
	IIL2	VIL2 = V_{SS}, V_{DD}=5.0V (when pulled-up)	- 200	- 100	- 20		

*1 : When the one terminal output state.

DC CHARACTERISTICS (4/4)

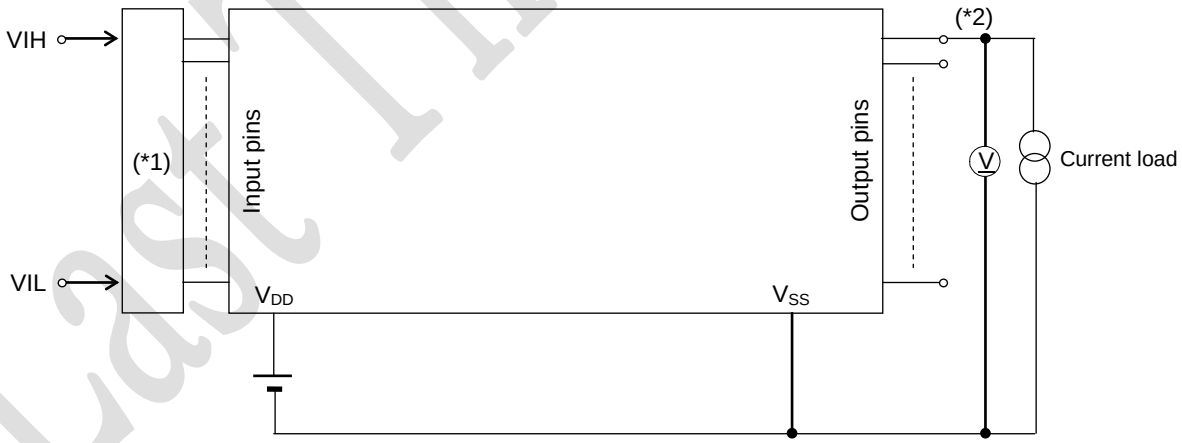
(V_{DD}=2.7 to 5.5V, V_{SS}=0V, Ta=- 40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit	Measuring circuit
			Min.	Typ.	Max.		
Input voltage 1 (RESET_N) (TEST) (PA0 to PA2) (PB0,to PB7)	VIH1	¾	0.7 ´ V_{DD}	—	V_{DD}	V	2
	VIL1	¾	0	—	0.3 ´ V_{DD}		
Input pin capacitance (PA0 to PA2) (PB0 to PB7)	CIN	f = 10kHz Ta = 25°C	—	—	20	pF	¾

MEASURING CIRCUITS

MEASURING CIRCUIT 1

MEASURING CIRCUIT 2

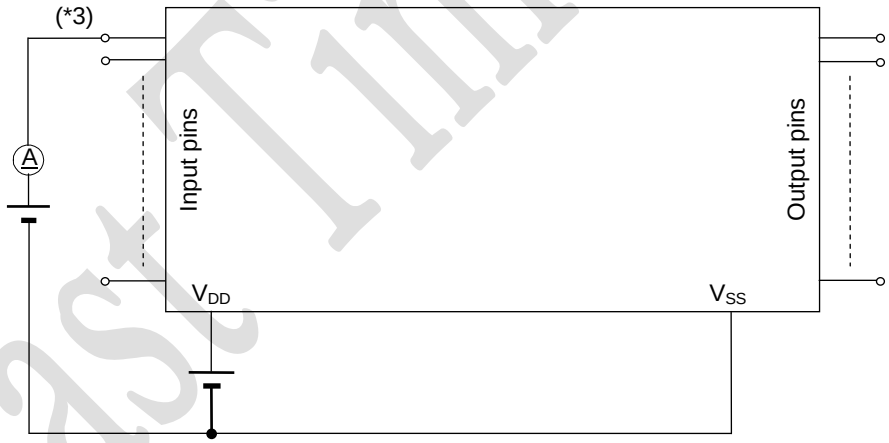


*1: Input logic circuit to determine the specified measuring conditions.
*2: Measured at the specified output pins.

MEASURING CIRCUIT 3

*1: Input logic circuit to determine the specified measuring conditions.
*2: Measured at the specified output pins.

MEASURING CIRCUIT 4

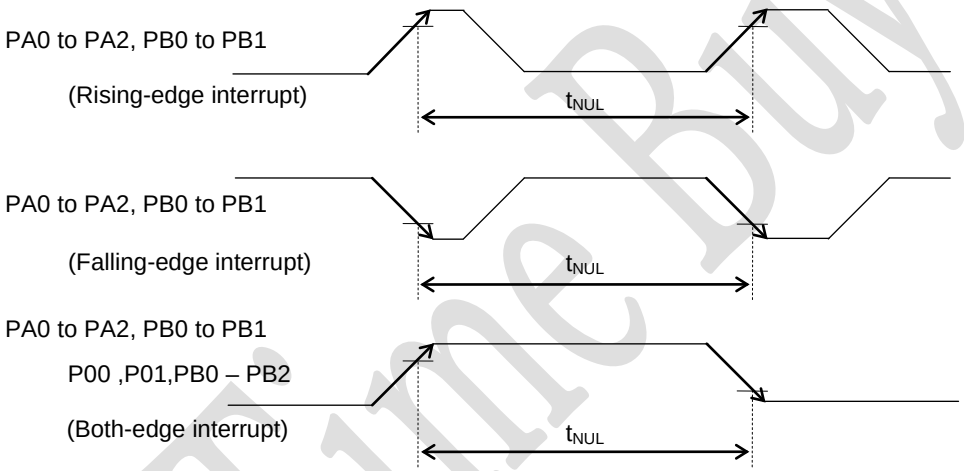


*3: Measured at the specified output pins.

AC CHARACTERISTICS (External Interrupt)

(V_{DD}=2.7 to 5.5V, V_{SS}=0V, Ta=- 40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
External interrupt disable period	T_{NUL}	Interrupt: Enabled (MIE = 1), CPU: NOP operation System clock: 32.768kHz	2.5 x sysclk	—	3.5 x sysclk	ms

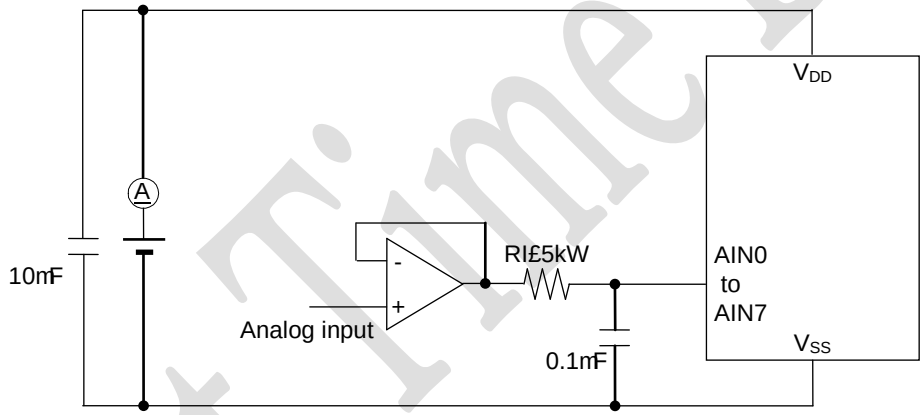


Electrical Characteristics of Successive Approximation Type A/D Converter

(V_{DD}=2.7 to 5.5V, V_{SS}=0V, Ta=- 40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Resolution	n	¾	—	—	10	bit
Integral non-linearity error	INL	R_I≦5kΩ，HSCLK=8.192MHz	- 4	—	+4	LSB
Differential non-linearity error	DNL	R_I≦5kΩ，HSCLK=8.192MHz	- 3	—	+3	
Zero-scale error	V_{OFF}	R_I≦5kΩ，HSCLK=8.192MHz	- 4	—	+4	
Full-scale error	FSE	R_I≦5kΩ，HSCLK=8.192MHz	- 4	—	+4	
Allowable signal source impedance	R_I	—	—	—	5k	W
Conversion time	t_{CONV}	¾	—	102	—	f /CH

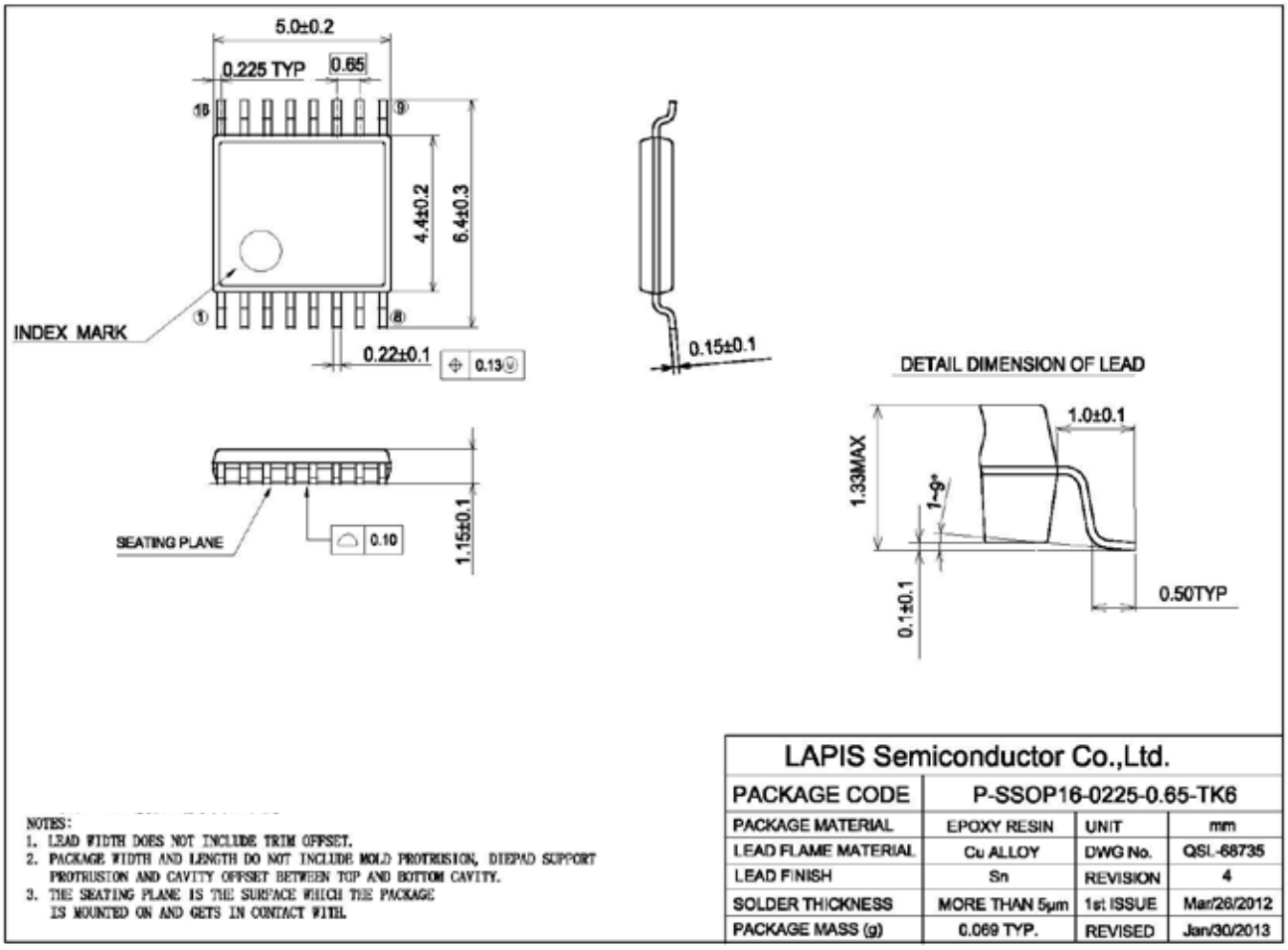
Φ : One cycle of OSCLK (F=3MHz or higher)



PACKAGE DIMENSIONS

ML610Q101/ML610Q102 SSOP16 Package

(Unit: mm)



NOTES:
1. LEAD WIDTH DOES NOT INCLUDE TRIM OFFSET.
2. PACKAGE WIDTH AND LENGTH DO NOT INCLUDE MOLD PROTRUSION, DIEPAD SUPPORT PROTRUSION AND CAVITY OFFSET BETWEEN TOP AND BOTTOM CAVITY.
3. THE SEATING PLANE IS THE SURFACE WHICH THE PACKAGE IS MOUNTED ON AND GETS IN CONTACT WITH.

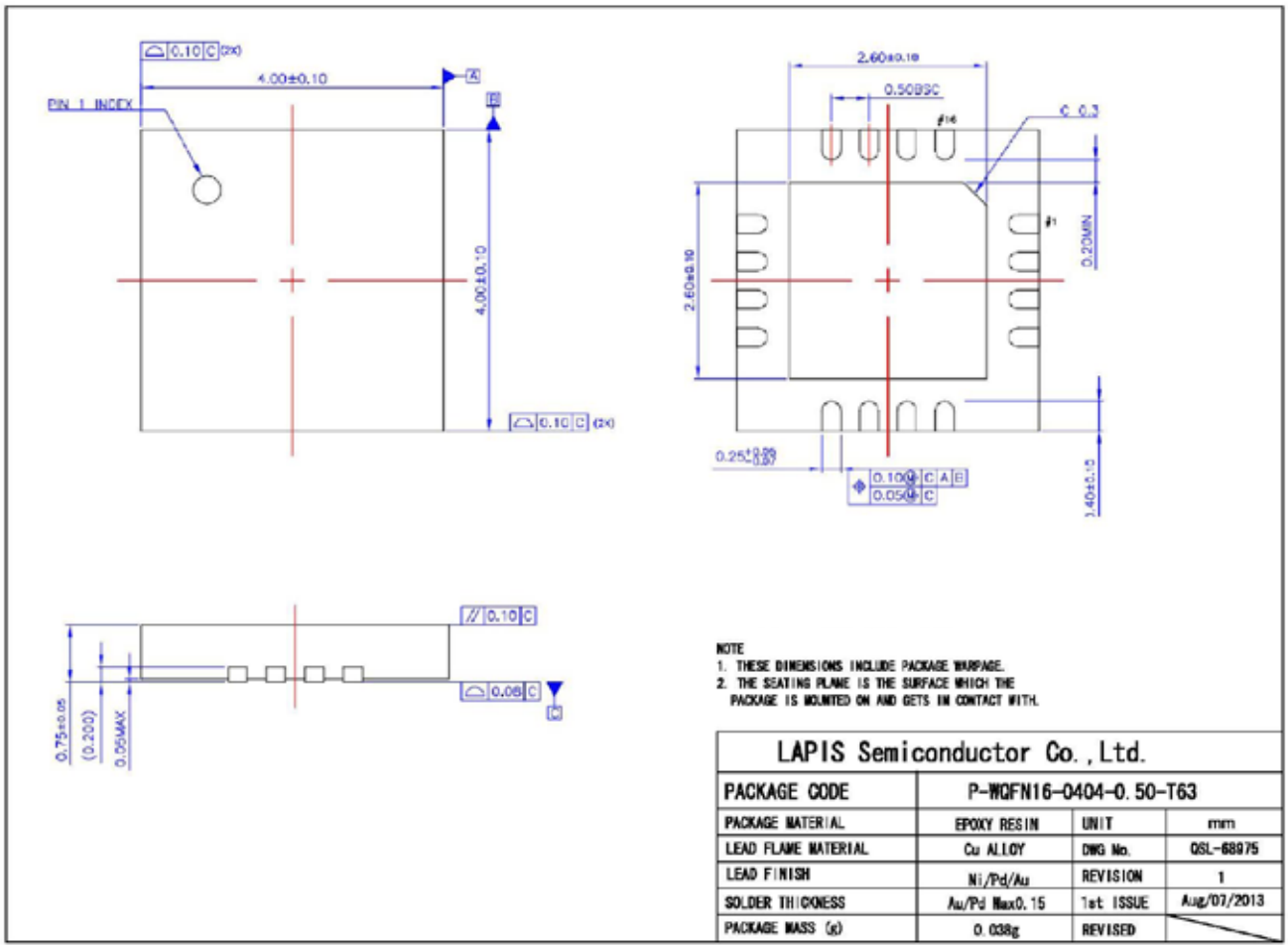
LAPIS Semiconductor Co.,Ltd.			
PACKAGE CODE	P-SSOP16-0225-0.65-TK6		
PACKAGE MATERIAL	EPOXY RESIN	UNIT	mm
LEAD FLAME MATERIAL	Cu ALLOY	DWG No.	QSL-68735
LEAD FINISH	Sn	REVISION	4
SOLDER THICKNESS	MORE THAN 5μm	1st ISSUE	Mar/26/2012
PACKAGE MASS (g)	0.069 TYP.	REVISED	Jan/30/2013

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact a ROHM sales office for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

ML610Q101/ML610Q102 WQFN16 Package

(Unit: mm)



Notes for Mounting the Surface Mount Type Package

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REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDL610Q101-01	Jan., 2013	–	–	Formal edition 1
FEDL610Q101-02	Aug., 2013	–	3	Added “16-pin plastic WQFN”
		–	7	Added ML610Q101/ML610Q102 WQFN16 Pin Layout
		6	8	Added PIN No. (SSOP)
		6	8	Changed the following description of PA0, PA1. “Input port” to “Input/output port”.
		18	19	Changed the following description. “f : f_{PLL}/4” to “f : f_{PLL}/2”
		18	19	Add ML610Q101/ML610Q102 WQFN16 Package
FEDL610Q101-03	Aug.4, 2015	–	–	Change the logo and style.
		19	19	Add the following items. “Allowable signal source impedance”
		13	13	Add the following items. “Power-on reset activation power rise slope”
FEDL610Q101-04	Dec 5, 2018	1	1	Changed “One-shot timer mode” to “One-shot mode.”
		2	2	Changed “One-shot PWM mode” to “One-shot mode.”
		12	12	Added the note *2.
		13	13	Corrected “1024 clock average” to “2048 clock average” in the note *1.
		13	13	Add the note *3 to the condition of “AC CHARACTERISTICS (Power on / Reset sequence)”
		19	19	Corrected the explanation of Φ : One cycle of OSCLK (F=3MHz or higher).

Notes

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